(11)Publication number : **10-304004**
(43)Date of publication of application : **13.11.1998**

(51)Int.Cl. H04L 29/02
H04L 29/08

(21)Application number : **10-095147**
(22)Date of filing : **04.03.1998**

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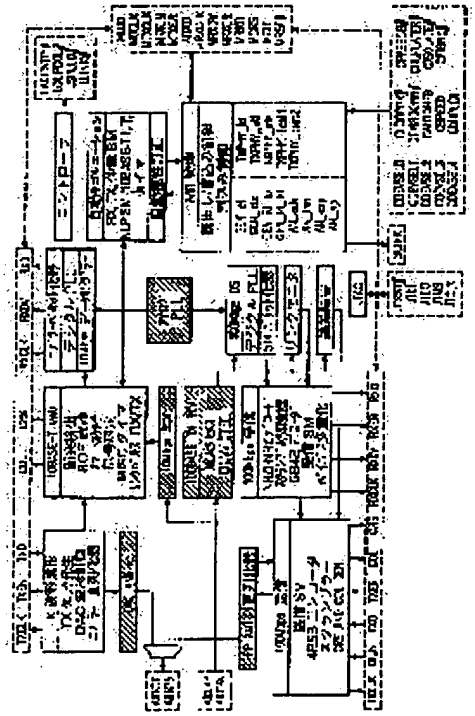
(30)Priority
Priority number : **97 38577** Priority date : **04.03.1997** Priority country : **US**

(54) IMPROVED PHYSICAL LAYER INTERFACE DEVICE



(57)Abstract:
PROBLEM TO BE SOLVED: To operate the interface at both reception and transmission transfer rates in a flexible mode by controlling the interface so as to decide an operating mode and selecte a proper receiver from a 1st and 2nd receiver, and/or select a proper transmitter from a 1st and 2nd transmitter.
SOLUTION: A signal chip 10 BASE-T/100 BASE-TX physical interface (PHY) includes a media independent interface connecting to a standard media access controller, its operation is controlled by using an internal register, and an automatic polarity correction circuit ensures immunity with respect to inversion of reception pair wires in the 10 BASE-T operating mode in the case of automatic selection. The PHY supports a single transmission/reception transformer connecting to a single RJ 45 connector at both operating speeds, includes an internal loopback circuit for a system test for both modes, and both the 10 BASE-T/100 BASE-TX support the full duplex transmission.

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram which the physical layer interface device of this invention simplified.
[Drawing 2] It is the block diagram which interconnection with the external configuration element of the physical layer interface device of drawing 1 simplified.

[Drawing 3] It is the figure which the formation of automatic negotiation composition for the physical layer interface device of drawing 1, state waveforms, and timing simplified.
[Drawing 4] It is the block diagram which the register of the basic set used in the physical layer interface device of drawing 1 simplified.
[Drawing 5] Drawing 5 A and drawing 5 B show the figure which MII read-out and writing simplified, respectively.
[Drawing 6] It is the figure which the signal name relevant to the bit position and each bit position for general-purpose control register GENctl simplified.
[Drawing 7] It is the figure which the signal name relevant to the bit position and each bit position for general-purpose status register GENsts simplified.
[Drawing 8] It is the figure which the signal name relevant to the bit position and each bit position for general-purpose identifier register GENidhi/GENidlo simplified.
[Drawing 9] It is the figure which the signal name relevant to the bit position and each bit position for the automatic negotiation public announcement register ANadv simplified.
[Drawing 10] It is the figure which the signal name relevant to the bit position and each bit position for the automatic negotiation link partner capability register ANlpa simplified by drawing 10 A, drawing 10 B, and drawing 10 C.
[Drawing 11] It is the figure which the signal name relevant to the bit position and each bit position for automatic negotiation expanded register ANexp simplified.
[Drawing 12] It is the figure which the signal name relevant to the bit position and each bit position for automatic negotiation following page transmission register ANnp simplified.
[Drawing 13] It is the figure which the signal name relevant to the bit position and each bit position for TLAN PHY identifier quantity / low register TLANYid simplified.
[Drawing 14] It is the figure which the signal name relevant to the bit position and each bit position for TLAN PHY control register TLPHYctl simplified.
[Drawing 15] It is the figure which the signal name relevant to the bit position and each bit position for TLAN PHY status register TLPHYsts simplified.
[Drawing 16] It is the figure which the signal name relevant to the location of the pin and each location of the pin for the physical layer interface device of drawing 1 simplified.
[Drawing 17] It is the block diagram which the 100BASE-TX receiver of the physical layer interface device of drawing 1 simplified.
[Drawing 18] It is a block diagram of the 100BASE-TX receiver of the physical layer interface device of drawing 1.
[Drawing 19] They are some more detailed figures of the 100BASE-TX receiver of drawing 18.
[Drawing 20] It is the block diagram which some 100BASE-TX receivers of drawing 18 simplified.
[Drawing 21] They are some more detailed figures of the circuit shown in drawing 20.
[Drawing 22] They are some more detailed figures of the circuit shown in drawing 20.
[Drawing 23] They are some more detailed figures of the circuit shown in drawing 20.
[Drawing 24] Although shown in drawing 17 and drawing 18, some detailed circuits of a high-speed comparator [like] are shown.
[Drawing 25] It is the block diagram which interconnection with a transmitter current source, external transmission machine load resistance, and an external isolation transformer simplified.

[Drawing 26] It is the block diagram which the circuit which makes a transmitter current source one gradually for control of rise time simplified.
[Drawing 27] It is the block diagram which the circuit which gives the high precision reference current for using it in a 100BASE-TX transmitter circuit simplified.
[Drawing 28] The detailed circuit of the preferred embodiment which realizes the circuit shown by drawing 27 is shown.
[Drawing 29] It is the block diagram which the circuit using the single input frequency which makes double DPLL speed possible simplified.
[Description of Notations]
1700 100BASE-T differential line receiver
1701 Capacitor
1702 Input line
1703 Capacitor
1704 Input line
1705 Capacitor
1706 Resistance
1707 Capacitor
1708 Resistance
1709 Resistance
1710 Resistance
1711 Resistance
1712 Voltage control amplifier
1712a Adjustable gain amplifier
1712b Adjustable gain amplifier
1712c Adjustable gain amplifier
1713a Equalizing circuit
1713b Equalizing circuit
1713c Equalizing circuit
1714 Peak voltage amplifier
1715 Capacitor
1716 Peak voltage amplifier
1718 Return signal
1718a Return
1718b Return
1718c Return
1720 Operational amplifier
1722 Reference voltage
1724 Amplifier
1726 Resistance
1728 Resistance
1730 Operational amplifier
1732 Reference voltage
1734 Capacitor
1736 Capacitor
1738 Comparator
1740 Data output

1800 100BASE-T differential line receiver
1802 Circuit generating reference voltage
1804 Line
1806 Square
1808 Resistance / capacitor circuit network
1810 Resistance / capacitor circuit network
1812 Resistance / capacitor circuit network
1814 Oscillator
1816 Frequency deciding circuit
1818 Phase locked loop
1820 Capacitor
1822 Control signal

[Detailed Description of the Invention]

[0001]
[Field of the Invention] This invention generally relates to details more about digital communications at a physical layer interface device.

[0002]
[Description of the Prior Art] A local area network (LAN) is accepted widely. Interconnection of many workstations and/or personal computers (PC) is carried out. It is used in many and the various industrial worlds by the mode which enables it to share data and a resource like APIRIKESHON without the necessity that they do not need an expensive mainframe computer but attach the terminal of the related large number again. The composition of one LAN accepted widely is registered trademark "Ethernet" LAN defined by IEEE802.3 standard.

[0003] LAN is accepted broadly, progress of art continues taking for accelerating, and the request of LAN configuration which has a quicker transfer rate is continuing increasing. Two sorts of 100 Mbyte/second (Mbps) LAN are having the range of the installing base of 10Mbps Ethernet LAN spread around. Although this increase of a transfer rate is desirable, this will be an occasionally big burden in much more expensive new 100Mbps equipment replacing real 10Mbps equipment. However, a certain kind of LAN can be run with dimorphism-type equipment [installation] . It will become convenient if it has a physical layer interface device which operates with both transfer rates.

[0004]
[Problem(s) to be Solved by the Invention] SUBJECT of this invention is advantageous in cost, and is providing the LAN physical layer interface device which can operate with both transfer rates in a flexible mode.

[0005]
[Means for Solving the Problem] This invention gives single chip double function 10BASE-T / 100BASE-X physical layer interface device compatible with real 5V part part. This PHY includes media a non-depending interface (MII), and connects it to a non-

covering twisted pair cable via an isolation transformer and RJ45 single connector. This PHY includes a built-in automatic negotiation circuit in which auto select of all the /half-duplex 10BASE-T and 100BASE-TX is made to perform, and an automatic polarity correcting circuit secures immunity performance to receiving pair line reversal in 10BASE-T operational mode in the case of that auto select. Although this PHY contains including an internal PLL circuit, 20 MHz clocks, i.e., a crystal, with this single, it suits both of the operational modes. This PHY contains low electric power (low power) and electric power downward (power down) mode. A 10BASE-T portion of this PHY contains a smart squelch for the improved receiving noise margin. This PHY includes a high jitter tolerance clock recovery circuit and a transmitting Java detector circuit. A 10BASE-T portion of this PHY includes an on-board transmission waveform forming circuit. A 100BASE-X portion of this PHY includes a synthetic rise time control circuit for decreasing an electromagnetic interference (EMI). This PHY includes a programmable transmission voltage amplifier for generating 100BASE-X-MLT-3 waveform, and a baseline wandering correction (DC recovery) circuit for a 100BASE-X receiver.

[0006]
[Embodiment of the Invention] If the following statements are considered in relation to an accompanying drawing, he will be able to understand this invention more clearly. A number and a sign corresponding with various figures shall express the part part which corresponds if there are no other directions.

[0007] Here, if drawing 1 is referred to, the block diagram which the physical layer interface device (PHY) of this invention simplified is shown there. this invention gives single chip 10BASE-T / 100BASE-X physical layer interface device (the following, 10/100PHY -- or it is only called PHY) so that he can understand from drawing 1. Drawing 1 also shows various signals which are supplied to the block of the versatility of PHY of this invention, or are supplied by these blocks again, and those interconnection states.

[0008] Say simply and PHY of this invention includes media the non-depending interface (MII) for making it make it connect with a standard media-access-control (MAC) device easily, In that case, connection with a non-covering twisted pair cable is made by the easy isolation transformer and RJ45 single connector (refer to drawing 2). PHY of this invention does not need the external elements for filtering or rise time control, but is contained on the chip of all the equalization elements. Operation of this device is a pin level by a composition-ized pin, or is controlled using a management data interface and an internal register. An automatic polarity correcting circuit secures the immunity performance to receiving pair line reversal in 10BASE-T operational mode including a built-in automatic negotiation circuit for this device to make the auto select of half a/full-duplex 10BASE-T and 100BASE-TX perform in the case of that auto select.

[0009] PHY of this invention shown in drawing 1 preferably, 3.3V power supply. The thing of the CMOS design which it has. (This 2 pin management interface.) the thing of the part part of 5V of the actual existence which has standard IEEE802.3u media the non-

depending interface (MII) which it had -- being compatible -- single package double function 10BASE-T / 100BASE-X physical layer interface device to be used are given. This PHY has composition-ized the IEEE802.3u automatic negotiation provided with the following page support function. This PHY supports the single transmission / reception transformer connected to RJ45 single connector to both working speeds. Only the quantity of the external elements minimum in the state where all the filtering and equalization elements were integrated to the device needs this PHY. This PHY includes the circuit for the internal loopbacks for doing a system test in both the modes, and contains the IEEE standard 1149.1 examination access port (JTAG). This PHY makes connection with CAT3 cable (10BASE-T) or CAT5 (10BASE-T, 100BASE-X) make, and uses insulating transmission / received power supply for the minimum combination. Although this PHY includes the internal PLL circuit using single 20-MHz clock, i.e., crystal, this suits both of the speed modes. This PHY contains low electric power (low power) and electric power downward (power down) mode, and supports full-duplex transmission by both 10BASE-T and 100BASE-X.

[0010] The 10BASE-T portion of this PHY contains the smart squelch which gives the receiving noise margin which follows IEEE802.3 thoroughly and was improved. This PHY includes the digital phase lock loop and transmitting Java (jabber) detector circuit of the DSP base which give big jitter tolerance clock recovery. The 10BASE-T portion of this PHY includes the on-board transmission waveform shaping function, without needing only an external terminal element, and includes the automatic polarity (reverse polarity connection) circuit.

[0011] The 100BASE-X portion of this PHY follows thoroughly the ANSI twisted pair Physical Medium Dependent (TP-PMD) and the IEEE802.3u standard, For this reason, an external capacitor is not needed including the synthetic rise time control facility for decreasing an electromagnetic interference (EMI) for EMI control. This PHY contains the receiver and transmitter which have the adaptive equalization circuit and the integrated baseline wandering correction (DC recovery) circuit which were integrated and which were integrated, including the programmable transmission voltage amplifying function for MLT-3 waveform generating. This PHY enables operation by the twisted pair length up to 0 to 100 meters, and includes the transmitting interception function for a true silence line state.

[0012] Drawing 2 shows the interconnection state of PHY of this invention provided with external elements. The differential line driver of 10/100PHY is designed drive CAT3 (or CAT5) cable which exceeds 100 m for CAT5 at least 100-m cable in 10BASE-T mode in 100BASE-TX mode again. As shown in drawing 2, three transmission output pins (AXMTP, AXMTN, and centre tap terminal area ACT) interface with borough (Valor)PT4171S single transformer (or equivalent device) in both operational modes. Thereby, the external connection to RJ-45 single socket by which direct continuation is carried out to the secondary winding of this transformer is simplified.

[0013] This 10/100PHY have incorporated the on-chip corrugating part for 10BASE-T transmission, and the rise time control section for 100BASE-TX transmission, The device

enables it to interface with a coupling transformer directly, without needing any external elements other than two terminators shown in drawing 2.

[0014] When drawing 1 is referred to here, there A 10BASE-T transmitter portion, Although it does not limit to a suitable transmission medium, for example, this, in order to transmit via a twisted pair, the digital pair analog (DAC) transmitting (DAC XMT) portion which changes the digital output of a transmitter block into an analog signal is shown. The 100Mbps transmitter portion which gives an output to the serialization machine block connected to the parallel transmitting (PPXMT) portion is also shown.

[0015] 10Mbps transmitter has a corrugating portion which takes out the data which should be transmitted (it is made the gestalt which transmits data) and which works like and tries a data stream (TXD) according to a ready-for-sending ability-ized signal (TXEN) in order to transmit via a transmission medium. 10Mbps transmitter gives a DAC waveform control signal, and has a NIBURA (nibbler) serialization machine. This block of a transmitter gives a transmit-clock signal (TXCLK) to the device which supplies a data stream, and a device has a right clock for a transmitter.

[0016] Similarly, the 100Mbps transmitter has the transmit-clock output signal (TXCLK), collision output signal (COL), and career sensing output signal (CRS) which are given to the device which supplies a data stream. A 100Mbps transmitter receives a data stream (TXD), a ready-for-sending ability-ized signal (TXEN), and a transmission error signal (TXER) from the device which supplies a data stream.

[0017] As shown in drawing 2, two receiver input pins (ARCVP and ARCVN) of 10/100PHY must be connected to the transmission line by which the termination was appropriately carried out via the external isolation transformer (this is the same as the transformer used for the transmitting portion of PHY). The single receiver input wire twisted pair line supports both speed modes, and all the multiplexing functions are performed inside a device.

[0018] A receiver circuit establishes the common mode input bias voltage of itself, and does not need an external resistance-type potential divider network. An easy external termination circuit network as shown in drawing 2 which consists of two resistance and one capacitor is preferred now. The data which received from this network is outputted to the MRXD nibble of MII synchronizing with the rising edge of a corresponding MRCLK signal. MRCLK frequency is automatically adjusted by 25 MHz in 2.5 MHz and the 100BASE-X mode in 10BASE-T mode.

[0019] If drawing 1 is referred to here, the 10BASE-T receiver has incorporated the smart squelch function to have only the function to pass ingress data, when a pulse sequence with it is received. [input amplitude larger than the minimum signal threshold level and and] [specific] This is protected so that impulse line noise may not check the activity of a signal or a link. This squelch circuit performs a quick stall, when a substandard pulse is received. A very long pulse is not made to malfunction like a link pulse.

[0020] The 100BASE-TX receiver shown in drawing 1 includes the circuit required in order to decode MLT-3 waveform (decoding) and to give a data nibble to a MRXD (0-3) pin. If a device receives MLT-3 signal, this signal will be amplified immediately and equalization will be carried out. This enables reception with CAT5 cable over 100 m. The low frequency components of MLT-3 signal are removed (in the transformer coupling circuit, it may have produced as a result of delay having no transient and long, and this ingredient is occasionally called wandering of the baseline). Subsequently, this MLT-3 ideal signal is internally changed into NRZI, and resynchronization is carried out to the clock with which itself was recovered using digital phase lock loop art after that. Subsequently, as for reverse, the data by which re-crocking was carried out is serialized by 5 bit-code groups, a releasing scramble is carried out to them, and the 5 B4B decipherment (decoding) of it is done. If the start of a stream delimiter (delimiter) is detected in 5B data stream, a following frame will be outputted to MII.

[0021] Both 10Mbps receiver (10Mbps RCV) block and a 100Mbps receiver (100Mbps RCV) receive a signal from a transmission medium so that I may be understood from drawing 1. The signal from 10Mbps block is given to control block (10BASE-T MAU), Although this control block does not plan to evaluate an input signal, for example, to limit it to this, it works so that the selected functions, such as a smart squelch and signal quality error (SQE) examination, signal authorization, and collision detection, may be performed. This control block gives collision detection (COL) and a career sensing signal (CRS) to a certain device which receives a certain data stream which carries out ingress via a transmission medium. This block samples data, before supplying data (RXD) and its clock signal (RXCLK) to a device, An input signal is given to other blocks which synchronize with a data clock and form PLL into a nibble packet (this supplies a received-data effective (RXDV) signal to a device again).

[0022] The 100Mbps receiver (100BASE-TX RCV) block of drawing 1 equalizes an input signal to the length of the transmission medium which performed baseline wandering correction and transmitted the signal. This receiver block gives received data to the 1st control block that performs a data sampling, the formation of 5B package, and the synchronization with digital PLL. Subsequently, the signal carried out in this way is given to the 2nd control block that performs NRZI-NRZ decipherment (decoding), releasing scramble, and 5 B4B decipherment and bypass multiplexing, including a receive state machine. The signal from the 1st control block is also given to a link monitor and an far-end failure detecter. The input signal processed as mentioned above from the 2nd control block is given to a device as received data (RXD) with a receiving data clock (RXCLK), data receiving data validity (RXDV), and a receiving error (RXER) signal.

[0023] An automatic negotiation block, the analog PLL block, the LED controller block, the MII management block, and the JTAG block are shown in drawing 1.

[0024] An LED controller block gives a suitable signal to LED which may be used in order to direct the state of operation of PHY. 10/100PHY -- "activity (ACTIVITY)" -- "-- duplex (double) one/collision (it has four pins designed drive LED for

DUPLEX/COLLISION", "link (LINK)", and "speed (SPEED)".) In a circuit, LED must be connected to digital one 3.3V via a current limiting resistor including the open drain NMOS device for a LED driver. It depends for the value of this resistance on the form of LED.

[0025] Link LED is turned on when PHY establishes an effective link in 10BASE-T mode. In 100BASE-TX mode, it directs to be in the state where a releasing scramble machine locks to data, and 10/100PHY can transmit and receive data. According to page reception, the flash plate of the link LED is carried out between automatic negotiations. Since this takes several seconds for an automatic negotiation process being completed, it gives a user directions of the activity of a link.

[0026] Activity LED is turned on when PHY has transmitted and received data. This LED is turned on during the minimum duration for 20 ms to each activity. The operation is the same at both speed modes.

[0027] When PHY is in full-duplex mode, the light is switched on continuously, and duplex one / collision LED is turned on during the minimum duration for 20 ms, when a collision arises in half-duplex mode. In continuation or an intermittent collision, the flash plate of this LED is carried out at 10 Hz.

[0028] Although it is in 10BASE-T, when there is nothing in automatic negotiation mode (after-mentioned), 10/100PHY sends out the link pulse from which only the period of 16 milliseconds (ms) was separated to a data output (DO) circuit.

[0029] A receiver looks for the effective link pulse in the input wire twisted pair line. When a link pulse is not received within the predetermined time period, a device goes into a "link failure" state. In this state, a link pulse continues being generated and a receiver continues looking for a link pulse pattern continuously. Preferably, PHY stops at this state until an effective receive packet or many regular link examination pulses are received. The link pulse of reverse polarity is also received and authorized in the same mode as the usual link pulse. This is used in order to give directions of inside reconstruction-ization of automatic having arisen in order to reverse receiving pair line connection and to correct this problem. In 100BASE-TX mode in which data is coded MLT-3, reverse polarity correction is unnecessary.

[0030] The automatic negotiation block contains the reception for transmission and control of a receiving block, transmission, and a mediation state machine (SM). This block contains a timer and a NLP state machine again. It is connected to a MII block and it performs automatic polarity correction.

[0031] 10/100PHY supports thoroughly an IEEE802.3u automatic negotiation including the following page transmission. If it becomes usable, 10/100PHY can perform a negotiation with this function by PHY in which other arbitrary automatic negotiations are possible, and its link segment, and those common highest protocols can be established. It does not express "LINK" until a certain PHY completes the negotiation. Much more

details of link partner capability may be made to be acquired by reading the data of 10 / 100PHY register.

[0032] Between loopback modes, all the receiving activities other than a link examination pulse are made incompetent for 10BASE-T mode. However, squelch information is still processed and it can be made to be maintained in a link condition under an instant loopback self test.

[0033] This PHY has composition-ized the perfect automatic negotiation standard containing the following page capability. The three pins CAUTONEG, CSPEED, and CDUPLEX are used in order to form a link rate into direct composition, or in order to set up and report the speed which carried out the automatic negotiation. Drawing 3 shows the automatic negotiation signal wave form to these three signals and a SLINK signal.

[0034] When CAUTONEG is low [of negative description] , CSPEED and a CDUPLEX pin determine link frame formation. Both the pins of CSPEED and CDUPLEX give the default composition of full-duplex 100BASE-TX, when it has weak pull-up and is, without being connected.

[0035] Since the value of CSPEED and a CDUPLEX pin is latched to automatic negotiation logic, the rising edge of CAUTONEG is used. The external controller must suspend driving these pins within 1200 ms (maximum), after CAUTONEG serves as quantity.

[0036] This PHY starts a negotiation, shortly after CAUTONEG is expressed. 750 ms (minimum) of the last of an automatic negotiation is for ensuring stopping at the stability between the time when a link is proper with a hysteresis timer. PHY drives CSPEED and a CDUPLEX pin and it is made to make link frame formation direct during this time. An external controller latches the value of these two pins by the rising edge of a SLINK pin.
[0037] The external controller must not start either drive of CSPEED and CDUPLEX, while CAUTONEG serves as quantity.
[0038] Table 1 summarizes the meaning of the value latched from CDPEED and a CDUPLEX pin, when an automatic negotiation begins. Here, Yes and No express ** and no, respectively.
[0039]
[Table 1]

[0040] PHY performs internal reset to the first power up. The external reset circuit is unnecessary. However, operation of 10/100PHY is unfixed between 50 milliseconds (ms) after powering on.

[0041] At the time of operation, perfect reset of a device can be performed by making low the MRST# pin between the periods which are not than 50 microseconds (microsecond). Right operation of a device is not guaranteed between the periods for 50

ms after a MRST# pin serves as quantity of negative description.

[0042] The JTAG block follows IEEE standard 1149.1 including the usual JTAG port. A JTAG examination access port consists of five pins, and these are used in order to interface with the board in which it is installed in order to do a device and a boundary scanning examination in in-series.

[0043] Although this PHY does not plan to limit a MII management block to various MII functions, for example, this, it makes it possible to perform read-out, write-in control, and interrupt control. The MII management block contains two or more registers which accommodate standard MII information, and two or more registers for other purposes. Drawing 4 is a register map suitable now for PHY of this invention. Eight registers of the upper part of drawing 4 are general registers defined by the MII standard. The register shown by attaching the prefix letter of TX is a register peculiar to TI. Other registers may be used by PHY of this invention. All other registers are read with zero.

[0044] It acts to the receiving circuit which corresponds to a twisted pair I/O pin as much as possible so that it may approach as loopback of the sending circuit of this PHY energizing the CLOOPBK# pin of a device, or by setting a LOOPBK bit in a general-purpose control register (GENctl).

[0045] An IEEE802.3u MII in-series protocol makes possible PMD in which each device possesses the internal register (16 bit width) to 32 and which is [to 32] different. This 10-/100BASE-T PHY has the composition of two or more internal registers (those some are formed into the hard wire).

[0046] It is the logic 1, a default, i.e., the IDLE state, of the two wire MII. All the tri-state (tristate) drivers are made incompetent, and the pull-up resistor of PHY pulls a MDIO line in the logic 1. If other transactions occur, before initializing it, a station management entity sends the preamble sequence of 1 bit of a series of logic of 32 of MDIO with a cycle [/ 32 / of MDCLK] , The pattern which can be used in order that PHY may establish a synchronization is given. If a certain PHY has other transactions, before it will answer this, it supervises a series of 1-bit sequences of 32 of MDIO provided with the cycle [/ 32 / of MDCLK] . Drawing 5 A shows the frame format for MII read-out. Drawing 5 B shows the frame format for MII writing. The easy description of these MII(s) format field is as follows.

[0047] Start delimiter: The start of one frame is expressed by 01 patterns. This pattern ensures conversion which is in 0 and returns from the line state of the default logic 1 to 1.

[0048] Action code: The action code of read-out is 10 and the action code of writing is 01.

[0049] PHY address: A PHY address is 5 bits which makes the unique PHY address of 32 possible. The first PHY address bit transmitted and received is MSB of an address. A

10-/100BASE-T PHY address is set using zero to CDEVSEL4 pin.

[0050] Register address: A register address is 5 bits to which the address of the individual register of 32 can be made to be carried out within each PHY.

[0051] Turnaround: The idle bit time when a device does not drive a MDIO signal effectively reads in order to avoid a contention, and it must be inserted between the register address field of a frame, and a data field. Between read-out frames, PHY takes out 1 bit [0] towards during [MDIO] the bit time in front of a data field after an idle bit. This field consists of 1 bit [0] and 1 bit [1] following it between write-in frames.

[0052] Data: A data field is 16 bits. The first data bit transmitted and received is MSB of data payloads.

[0053] A pause / interruptible-ized cycle: A pause cycle is a cycle following data transfer, and both a MAC controller and PHY drive a MDIO pin in the meantime. By the next rising edge of MDCLK after a pause cycle, (MDC may be driven to LOW by PHY, in order that) between quantities and MDIO may direct similarly that PHY interruption serves as pending.

[0054] Drawing 6 shows the signal name relevant to the bit position and each bit position for general-purpose control register GENctl.Table 2 shows the bit, signal name, and function of this general-purpose control register.

[0055]
[Table 2]

[Table 3]

[Table 4]

[0056] Drawing 7 shows the signal name relevant to the bit position and each bit position for general-purpose status register GENsts.Table 3 shows the bit, signal name, and function of this general-purpose status register.

[0057]
[Table 5]

[Table 6]

[0058] Drawing 8 shows the signal name relevant to the bit position and each bit position for general-purpose identifier register GENidhi/GENidlo.

[0059] Drawing 9 shows the signal name relevant to the bit position and each bit position for the automatic negotiation public announcement register ANadv.Table 4 shows the bit, signal name, and function of this automatic negotiation public announcement register.

[0060]
[Table 7]

[Table 8]

[0061] Drawing 10 A, drawing 10 B, and drawing 10 C show the signal name relevant to the bit position and each bit position for automatic negotiation link partner capability register AN1pa.

[0062] Link partner capability register AN1pa has three different formats by when the page was received.The first page received from the link partner is always in the basic page coding (encoding) state, and is used by PHY for automatic-constitution-izing. When the link partner is supporting the following page swap, the page received succeedingly can be in the state of a message page or unformatted page coding either, and this is determined by the value of a LPMP bit. Table 5 shows the bit, signal name, and function of a basic page register. Table 6 shows the bit, signal name, and function of a message page register. Table 7 shows the bit-signals name and function of an unformatted page register. Table 8 shows the message code field of Table 4.

[0063]
[Table 9]

[0064]
[Table 10]

[0065]
[Table 11]

[0066]
[Table 12]

[Table 13]

[0067] Use of the following page is summarized as follows. Both PHY and a link partner direct the following page capability for starting exchange of the following page to one side. If both devices have following page capability, both devices must send at least one following page. The following page swap continues until it stops having a page beyond it which transmits so that every device on a link may be expressed by the LPNP/NP bit. If it stops having other information which a device transmits, the message page provided with the blank message code field value will be sent. If a message code has a specific message or an unformatted page (one or more than it) of a continuation, it can express the information which defines how it is interpreted. When a message code refers to an unformatted page, an unformatted page follows a reference message code immediately in the order specified as the message code. The user of an unformatted page has to have responsibility to controlling the format and sequence-izing for the unformatted page of the users, them.

[0068] Drawing 11 shows the signal name relevant to the bit position and each bit position for automatic negotiation expanded register ANexp.Table 9 shows the bit, signal name, and function of this automatic negotiation expanded register.

[0070] Drawing 12 shows the signal name relevant to the bit position and each bit position for automatic negotiation following page transmission register ANnp.Table 10 shows the bit, signal name, and function of this automatic negotiation following page transmission register.

[0072] Drawing 13 shows the signal name relevant to the bit position and each bit position for PHY identifier quantity / low register TLPHYid.This PHY identifier quantity / low register are 16 bit registers having contained the identifier codes specified by [for TLAN PHY/PMI] TI and which were formed into the hard wire. An additional identifier is required in order to identify non-IEEE802.3 PHY/PMI which otherwise is not supported depending on an IEEE802.3u MII standard. The identifier codes for internal 10 / 100BASE-T PHY are 0x0003. Drawing 14 shows the signal name relevant to the bit position and each bit position for PHY control register TLPHYctl.Table 11 shows the bit, signal name, and function of this PHY control register.

[0074] Drawing 15 shows the signal name relevant to the bit position and each bit position for PHY status register TLPHYsts.Table 12 shows the bit, signal name, and function of this PHY status register.

[0076] Drawing 16 shows the signal name relevant to the location of the pin and each location of the pin for 10/100PHY of this invention. In drawing 16, as the key, i.e., the guidance, to the prefix of a pin name, The power supply for digital logic or grounding, and A D The power supply or grounding for analog circuitry, Directions of a PHY state and A of an interface and S are connections with internal analog circuitry. [as opposed to / C / as opposed to / insides / LED and J / as opposed to / in the composition-ized mode and M / media non-depending interface connection / in L / JTAG-test ports / a fiber transmitter module in F] Table 13A - 13I shows various pins, signal names, and functions, and especially the table 13A A network interface pin, Table 13B an external configuration-ized pin and Table 13C An LED interface pin, Table 13D -- a medium non-depending interface pin and Table 13G express a JTAG test-ports pin, Table 13H expresses a special test mode interface pin, and, in Table 13I, an external status pin and Table 13F express [an external configuration-ized pin and Table 13E] a network interface pin.

[0086] Here, reference of drawing 17 shows there the block diagram which the 100BASE-T differential line receiver 1700 simplified. In details, the receiver 1700 has more the two input lines 1702 and 1704 which receive the differential signal inputs ARCVP and ARCVN. These two differential signal inputs are outputs from the external isolation transformer (not shown in drawing 17) which connects a transmission line to data resources (the signal from these data resources is received).

[0087] The receiver 1700 does not need an external resistance voltage divider circuit network so that I may be understood from drawing 2. Instead, the resistance-type potential divider network serves as the first portion of a receiver. This network consists of three resistance 1706, 1708, and 1710 arranged in the input line of a receiver. this network commits the voltage swing which this receiver circuit looks at so that it may decrease till the minute of the voltage swing seen when there is no resistor network half [

about] .

[0088] The differential signal from a voltage voltage divider circuit network is supplied to an adjustable gain amplifier (AGA) or the voltage control amplifier (VCA) 1712, and this works so that the signal may be reinforced for the loss produced through the transmission line at the time of transmission. Preferably, this enhancement is dependent on frequency (this is for the signal loss in a transmission line to be dependent on frequency and the length of a line). Two reinforced outputs from VGA rank second, and pass the peak voltage amplifiers 1714 and 1716, respectively.

[0089] The two peak voltage detectors 1714 and 1716 work so that two important functions may be performed. One function is determining the quantity of wandering of a baseline and enabling it to remove it. Other functions are that determine signal strength and it may be reinforced even to a right level by the return signal 1718 given to VCA1712. When long delay arises between signal level transition, wandering of a baseline may arise. The inductance of the transformer used in order to insulate a transmission line is low, If there is transition of the signal level which will make decrease it slowly and (attenuation will become larger as time is formed) continue if the signal of a constant level has it, in order to give "edge", more than it is needed for others, in order to drive a signal level, wandering of a baseline will produce it.

[0090] In order to compensate wandering of baseband, the output from the detectors 1714 and 1716 is given as an input to the operational amplifier (op amp) 1720. If the 1st detector 1714 has baseline wandering bias, it will measure the high level of the signal having contained it. Since an input signal is a differential signal, if the 2nd detector 1716 has wandering of a baseline, it will measure the high level of the negative signal having contained the bias from it. However, this high level is equivalent to the low level (namely, trough) of a signal which the 1st detector 1714 looks at. That is, the two detectors 1714 and 1716 measure the peak and trough (this is a peak versus the peak value) of a signal. Therefore, since a true baseline is the middle between a peak versus peak values, if there is wandering of a baseline, the bias from it can be compensated. The output of an operational amplifier is filtered by the capacitor 1734. The output from the operational amplifier 1720 may be measured with the reference voltage 1722 in the amplifier 1724, and if there is subsequently baseline wandering bias, in order to offset this, a suitable level control is performed to the input signal of VCA1712. In this mode, before a signal goes into an active circuit, wandering of a baseline is removed, VGA1712 is enabled to acquire a bigger controllability if needed, and the voltage level which VCA1712 looks at in the input with combination with the initial-voltage voltage divider of three resistance 1706, 1708, and 1710 is restricted.

[0091] If the thing of one another gestalt to this easy art in comparison carries out the reconstitution of the transmitted original signal, subsequently subtracts it from the Irikita signal and has wandering of a baseline, it will be determining that quantity. However, since this becomes a system of a positive feedback form as a matter of fact, it will lose control easily.

[0092] A part of output voltage from two peak detectors descends among one pair of resistance 1726 and 1728, The produced output voltage is given to other operational amplifiers 1730, is compared with the reference voltage 1732 there, and in order to control the amount of enhancement subsequently given by VCA1712, it is used as the return signal 1718 to VCA. The return signal 1718 is filtered by the capacitor 1736. Similarly, it depends for the amount of enhancement on frequency preferably. Preferably, it depends for the amount of enhancement on the length and frequency of a transmission line (namely, the amount of enhancement as a function of received signal strength changed as a function of frequency). This compensation is chosen so that high-frequency attenuation of the signal in alignment with a transmission line may be offset as line length's function. In this mode, the output of VCA1712 is adjusted so that it may become desired signal value within the limits to a desired frequency range. That is, it means that the transmitted original signal was transmitted with the known signal level which is specific accuracy within the limits. This enhancement gives an output signal from a receiver on the almost same level as the transmitted original signal to various frequency components.

[0093] The output from VCA1712 is further given to the comparator 1738, and the output of this comparator turns into the data output 1740. That is, although this signal is equivalent to the received input signal, it is preferably adjusted to the arbitrary signal losses which it is preferably adjusted to wandering of arbitrary baselines, and are produced at the time of transmission.

[0094] Here, if drawing 18 is referred to, the simplified block diagram of everything but the 100BASE-T differential line receiver 1800 is shown there. In details, this receiver has more the two input lines 1702 and 1704 which receive the differential signal inputs ARCVP and ARCVN. These two differential signal inputs are outputs from the external isolation transformer (not shown in drawing 18) connected to a transmission line.

[0095] A voltage voltage divider circuit network is a portion of the beginning of the receiver 1800, and this is made from the resistance 1706, 1708, 1709, and 1711 and the capacitors 1701, 1703, 1705, and 1707 so that he can understand from this block diagram. this network commits the voltage swing which this active receiver circuit looks at so that it may decrease till the minute of the voltage swing seen when there is no network half [about] .

[0096] The signal from a voltage voltage divider circuit network is given to two or more adjustable gain amplifiers (VCA) 1712a, 1712b, and 1712c, and these work so that the signal for specification frequency spectrum may be reinforced to the loss produced at the time of transmission in alignment with a transmission line. Although such three VCAs are illustrated, it may be used by VCA more than it or not more than it, making it such whether it is **, and, probably, is still within the limits of this invention. Each VCA bears the enhancement covering an assigned frequency band. In drawing 18, as for one VCA1712a, all the frequency is assigned, as for 2nd VCA1712b, the frequency (1-20 MHz) of the middle range is assigned, and, as for 3rd VCA1712c, the frequency (20 MHz and more than it) of the high range is assigned. It is designed compensate selectively so

that the output of each VCA may be supplied to the equalizing circuits 1713a, 1713b, and 1713c and these may compensate the line loss of the specification frequency spectrum of the VCA.

[0097] As shown in drawing 18, the actual amounts of enhancement may differ with each frequency band. That is, 1st VCA1712a for the whole frequency range has the return 1718a of fixed quantity so that enhancement may not be given to an input signal. 2nd VCA1712b (intermediate frequency) has the amount of return 1718b based on the feedback circuit 1730. 3rd VCA1712c (high frequency) has the return based on the square (1806) of the feedback circuit 1730. Therefore, comprehensive enhancement and equalization are dependent on frequency. Two differential outputs from each equalizer circuits 1713a, 1713b, and 1713c rank second, it is added to a pair of single output, and each compound output is sent to the peak voltage detectors 1714 and 1716 after that.

[0098] The two peak voltage detectors 1714 and 1716 work so that two important functions may be performed. One function is determining the quantity of wandering of a baseline and enabling it to remove this. Other functions are that determine signal strength and it can be made to be reinforced even to a right level by the returns 1718a, 1718b, and 1718c to VCA. Although these functions are as having mentioned above, the additional circuit element is shown.

[0099] The added output from an equalizer circuit is further given to the comparator 1720. This output 1740 is data output NRZOUT. That is, this signal will be preferably adjusted to it, if there is wandering of a baseline, it will be preferably adjusted to this and signal loss will arise at the time of transmission, although it corresponds to a received input signal.

[0100] Here, when it returns to the equalizing circuits 1713a, 1713b, and 1713c shown in drawing 18, it turns out that each circuit is connected with resistance / capacitor (RC) networks 1812, 1810, and 1808 in order to determine the amount of equalization as a function of frequency, respectively. The control signal 1822 is supplied to these RC networks, and the resistance of resistance (one or more than it) of a network is controlled. A certain equalizing circuit may also contain only a capacitor and does not need to supply a control signal to the circuit of only such a capacitor. A control signal is given with the output from the voltage controlled oscillator (VCO) portion 1818 of the phase locked loop (PLL).

[0101] The circuit generating reference voltage 1802 is similarly shown in the voltage voltage divider in the input of the receiver 1800 as a ** thing in output voltage via the line 1804. Suitable reference voltage is supplied to other portions of the receiver 1800 by the circuit 1802. The reference voltage in the oscillator circuit 1814 to which the frequency deciding circuit 1816 is attached is supplied, and the control signal 1822 is supplied also to this frequency deciding circuit 1816.

[0102] The three capacitors 1734, 1736, and 1820 are external capacitors attached to the pins ACBLW, ACAGC, and ACPLL, respectively.

[0103] Drawing 19 is one example of the RC network to each of three equalizer circuits of drawing 18. In detail, the 1st MOSFET (tn0) controlled by bias voltage RC is shown. It is said again that RC is an output from the VCO portion of PLL. Bias of this MOSFET (tn0) is carried out so that it may become a linear action range by RC, and it works as resistance for the 1st equalizer circuit (it has a certain peculiar capacity again). Two or more MOSFETs (tn1-tn17), two resistance (i0 and i1), and two pairs of capacitors (2i0, 2i1 and 2 i2, 2i3) form the RC network for the 2nd equalizer circuit.Finally, one pair of capacitors (2i4, 2i5) and resistance (i2) are the RC networks for the 3rd equalizer circuit.Controlled [and] by bias voltage RC so that MOSFET (tn1-tn17) also ensures operation of those proportional regions, they work as resistance for adjusting the frequency characteristic of an RC network. By making an RC signal the same as that of the thing of PLL, in order that MOSFET which can be adjusted may set up an equalization damping time constant correctly, it may be used (it is the same voltage used in order that this may set up MOSFET which can be adjusted by both VCO of an equalizer and PLL, and). It is because scaling of the capacitor may be carried out simply. This circuit shows what bias of the MOSFET may be preferably carried out in the process in inaccurate resistance, in order to give and maintain the bandwidth controlled correctly. That is, in order to define an equalization damping time constant, a transconductance is provided in the accuracy of a capacitor more exact than resistance.

[0104] Here, if drawing 20 is referred to, details are shown there from a part of those of drawing 18. It is shown how an oscillator block may be especially divided into those interconnection by oscillator subblock (OSC), voltage comparison block (vcocomp), and loess bias (resbias) blocking. Drawing 21 shows some detailed circuits of an oscillator subblock. Drawing 22 shows some detailed circuits of a vcocomp block. Drawing 23 shows the detailed circuit of a loess bias block.

[0105] In drawing 20, a CP signal is the cascode bias for p form MOSFET, and a control signal (CONTROL) is improvement in the speed or a signal for low-speed-izing about oscillator frequency. A CMX signal is common mode reference voltage, PD is an electric power downward (power down) signal, and NPD is non-electric power fall signals. REFP and REFN are p and n-type-transistors bias voltage, respectively. PRESBIAS and BNSUM are the bias voltage p for making pMOSFET into the straight-line (resistance) active region, and for n form MOSFET pairs, and RC is the generated bias output. OUTP is a square wave output clock signal.

[0106] Here, if drawing 21 is referred to, one pair of capacitors (2i0, 2i1) will form the core of an oscillator circuit, and they will be appropriately charged and discharged so that the positive output signal OUTP and the negative output signal OUTN may be given (these output signals are a sawtooth wave or a chopping sea).The current which flows through the transistors tn6 and tn7 is used in order to charge and discharge these capacitors. When one side increases only in the specified quantity, another side of the current of the transistors tn6 and tn7 is an opposite direction mutually, as only the

specified quantity decreases, namely, these current serves as push pull mode in order to charge or discharge a capacitor pair. When one transistor has charged one one side of the capacitors, another side has charged the side other than other capacitors.

[0107] In particular, fixed DC current flows into these two transistors, and this is mixed with the current from the transistors tn0 and tn4. When becoming enough that the current from the transistors tn6 and tn7 overcomes the static current from the transistors tn0 and tn4, a result by which the related capacitor is charged is brought. When insufficient for the current from the transistors tn6 and tn7 overcoming the static current from the transistors tn0 and tn4, a result by which the related capacitor is discharged is brought.

[0108] The transistors tn9-tn12, and tn19 and the common mode feedback circuit of tn20 which were connected to the OUTP line and the OUTN line are committed so that the central arrangement of the voltage swing of a capacitor may be carried out and it may be maintained about the fixed voltage CMX. The quantity of the current which flows through the transistors tn6 and tn7 is determined by two transistor pair tn16/tn18 and tn15/tn17, These transistor pair is made one or OFF by one pair of bias voltage (FBN, FBP) supplied by vcocomp block. These two signals are return signals from a vco comparison block (refer to drawing 22), and one side of a transistor pair is made one and they turn OFF another side.

[0109] REFP and REFN are fixed reference bias voltage which determines the current which flows through the transistors tn2 and tn3. in order for a control signal to be a signal from the phase-comparison portion of a PLL circuit, to change PLL frequency and to synchronize PLL and external clock speed -- the speed of charge of a capacitor, and discharge -- improvement in the speed -- or it works so that it may low-speed-ize. The bottom ** (NPD) signal of non-electric power is used in order to stop the bias of the remaining things of a circuit appropriately. Please mind that this circuit occurs and the RC signal used by the equalizing circuit at least is given suitable for other circuits of a receiver.

[0110] Here, if drawing 22 is referred to, some details of the vcocomp block of drawing 20 are shown. The differential signal (OUTN and OUTP) from the oscillator block of drawing 21 is supplied to this circuit by INP and an INN signal (high order end of a circuit). These signals are compared with REFP and REFN by the pair of further others by tn0, tn1, and tn2 and tn6, respectively. These pairs drive the ECL latch (tp3, tn13, tn12, tdum10, tn16, tn20, tn14, tn2, and tn23) who works so that it may lock in transition and a jitter-proof circuit may be given. This latch gives a differential square wave feedback output (FBP and FPN) to the oscillator of drawing 21 via other transistor pairs. A rail couple rail square wave voltage output is given by OUTP.

[0111] Here, reference of drawing 23 shows there some detailed circuits of the loess bias block of drawing 20. The half of the current of this circuit flows into p form MOSFET (tp3) and its leg, and other halves flow into p form MOSFET (tp1) and its leg. These two MOSFETs are working as load resistance. PRESBIAS and BNRES are used in order to set bias as these two FET and to put these on a linear action field. Since it consistents

with the voltage to which it corresponds for other FET similarly provided by outputting those gate voltage as BNRES, the drain/source voltage for FET (tn9 and tn15) are driven. That is, BNRES is the bias for n form "resistance" FET.

[0112] Here, if drawing 24 is referred to, the detailed circuit for a part of high-speed comparator which was used for drawing 17 and drawing 18 is shown there. This circuit uses PRESBIAS and a BNRES signal, in order to carry out bias of that FET appropriately so that load resistance may be given. Similarly, the difference inputs INP and INN are measured with BEFP and REFN, and give the differential output which swings a peak versus a peak to PUTP and OUTN. The transition time for input signal edge is about 4 seconds, and the transition time for a circuit is about hundreds to 5 pico seconds. The half of the current in a switching point flows through load FET (tp3 and tp2).

[0113] Here, if drawing 25 is referred to, the block diagram which interconnection with two symmetrical transmitter current source / sinks, external transmission machine load resistance and an external insulation, or a coupling transformer simplified is shown there. At the time of 10BASE-T operation, MOSFET works as a switch, is closed with the suitable gating signal from control logic, and connects the analog Vdd to the centre tap (ACT) of a coupling transformer. At the time of 100BASE-T operation, the suitable gating signal from control logic opens MOSFET, and it carries out connection release of the centre tap (ACT) of a coupling transformer from the analog Vdd.

[0114] At the time of 100BASE-T operation, one current sinking is turned on and lengthens Vdd to maximum current (it corresponds to +1) via the load resistance of the same side from a current sinking (load resistance of an opposite hand) via the load resistance in the coil of a transformer, and the opposite hand of the coil. Subsequently, this current falls to 0 and other current sources start that current ramp (it corresponds to -1) of an opposite direction via the coil of a transformer, and the load resistance of an opposite hand. Therefore, it accumulates in a non-zero waveform and only one current source is driven at once. Although a quantity current source is switched to one for a zero waveform, a current value is a half when they operate separately. This gives symmetrical and smaller more highly precise voltage swing.

[0115] At the time of 10BASE-T operation, one current sinking is turned on and lengthens maximum current via the half part by the side of the sink of the coil of a transformer from Vdd. Only tales doses (about 1.25V) move by transformer operation more than Vdd, and other half parts of a coil give the maximum voltage between the primary coils which carried out the main arrangement by Vdd. Subsequently, the current sinking of an opposite hand is turned on and pulls maximum current via the half part by the side of the sink of the coil of a transformer from Vdd. Similarly, this gives the maximum voltage between the whole coil. Thus, both current sources are driven by turns. This gives a high voltage output rather than accepting the lowness of the accuracy of the voltage which must have been permitted in the case of 100BASE-T.

[0116] In this mode, 10BASE-T / 100BASE-TX transmitter of combination use RJ45 single connector provided with the external switching transistor or the relay. The external

capacitor for giving a suitable damping time constant so that suitable switching may be secured, and resistance are unnecessary. To 100BASE-TX operation, a termination is carried out thoroughly, and this connection method makes symmetrical performance possible, and enables 10BASE-T operation of another side 3.3V.

[0117] Here, if drawing 26 is referred to, the block which the circuit which carries out there the stage arrangement of the transmitter current source appropriately using the signal from the recycle delay line which is a part of analog PLL circuit of PHY of this invention, and is made one simplified is shown. It is not influenced even if the device transconductance of a current source/sink which has the capacitor on chip connected to the gate changes, in order that they may control rise time, even if one and OFF of a transmitter current source change [mode / this] the accuracy of a component.

[0118] PLL contains two recycle delay lines in details more, one of these is chosen so that 10BASE-T operation may be given, and another side is chosen so that 100BASE-TX operation may be given. This PLL includes the usual phase detector circuit which measures a 20-MHz external clock signal and the output (dividing is appropriately carried out in order to make comparison meaningful appropriately) from one of a delay line, This suitable output is chosen by the multiplexer (mux) controlled by the control signal given by the block of control logic. Subsequently, a phase detector gives the output signal of the rise for increasing or decreasing the clock rate of a recycle delay line, or descent to a charge pump circuit, and this charge pump circuit adds an electric charge to the capacitor which goes up or descends the speed of the recirculation which met the delay line, or lengthens. However, a control signal is given to various multiplexers which this determines which delay line should receive a signal by giving these speed rise or fall signals to the block of a control circuit, and choose an output signal from a desired recycle delay line. Control logic gives a signal to the start-up part of the selected delay line, and it is made to make the start up perform.

[0119] The strobe signal from the output of various elements which constitute a delay line is given to two or more current sources. In drawing 26, such four current sources are shown as what was connected in parallel, and, as for these four current sources, one of the current sources of drawing 25 is expressed. It may be used for by the current source of the number not more than it beyond it, making it such. The strobe signal from the element of a delay line works so that the related current source may be made one (or OFF). It comes to give the rise time controlled even if the current source was made one in the delay stage and it did not use an external rise time control element in this mode, The capacitor (if the produced waveform is smoothed and a staircase arises, it will work so that it may decrease [whether it is removed and]) shown in such an element, for example, drawing 26, using this art can become on chip now. In the example of this invention suitable now, such four current sources are used, and it is made one by the delay for 1 nanosecond from one current source to other current sources so that all the current sources may be thoroughly turned on in 4 nanoseconds. That is, the suitable strobe from the element of a PLL delay line is given to each current source at intervals of 1 nanosecond.

[0120] Control logic gives the control signal which determines whether a current source one [a current source] or turns off and in which direction current is generated in a row to a current source. Although drawing 26 shows successive one (or OFF) of four current sources, one delay line can make them one sequentially whether it is **, and other delay lines can make all them one simultaneously. The rise time by which the element as which the desired delay line was chosen gave the strobe signal to the suitable current source as another mode, and the request was controlled may be made to be given. It may be used in order that arbitrary numbers of delay lines which equipped with arbitrary numbers of elements may control a preselected number of current sources selectively.

[0121] Here, if drawing 27 is referred to, the block diagram which the circuit which gives there the high precision reference current used for a 100BASE-TX transmitter circuit simplified is shown. Especially new use of control of the cascade gate voltage within a control feedback loop decreases the influence of the limited output impedance in a current mirror, without sacrificing voltage capability with the current source current of an output. To the usual reference current circuit, the current which flows through FET corresponding to FET T1 of drawing 27 will have the current I equal to what broke the voltage Vref by the value of the resistance R. However, if Va changes, when Va is not equal to Vb, I will change for the limited output impedance of T1 which changes I. The circuit of drawing 27 supervises Va and it is made for Vb to serve as the same voltage. In this case, I becomes what always broke Vref by R. When two FET is replaced to T1 of drawing 27, they restrict the level with which Va can go up, before FET of the two FET bottom begins to be come by off. In a current mirror circuit, the current I of drawing 27 may be preferably used so that the current source of drawing 25 may be given.

[0122] Drawing 28 shows the detailed circuit of the preferred embodiment which realizes the device shown by drawing 27.

[0123] Here, if drawing 29 is referred to, when clock recovery is performed there in digital one, the block diagram which the circuit using the single input frequency which makes DPLL speed possible to both 10BASE-T and 100BASE-TX simplified is shown. This circuit is using two delay lines, and use 2 dividing (/2) either the 6.25 dividing (/6.25) stage or the stage for a PLL feedback loop, and this, Comparison speed and loop band width can be made to be held highly enough so that not external elements but an internal loop filter element can be used.

[0124] although this invention was indicated in relation to the graphic display example, this statement is interpreted in the restrictive direction -- as -- it is not meant. If various change of a graphic display example and other examples of this invention refer to this statement, it will be becoming clear to a person skilled in the art. Therefore, a claim thinks that such arbitrary change or examples that are within the limits of the truth of this invention are included.

[0125] The following paragraphs are further indicated about the above explanation.
In a physical layer interface device, (1) The 1st receiver for the 1st operational mode, The 2nd receiver for the 2nd operational mode, and the 1st transmitter for the 3rd operational

mode, A physical layer interface device possessing the control circuit which determines operational mode as the 2nd transmitter for the 4th operational mode, chooses a suitable receiver from the 1st and 2nd receivers of the above, and/or chooses a suitable transmitter from the 1st and 2nd transmitters of the above.

[0126] (2) A physical layer interface device including further the connection circuit for connecting this physical layer interface device to a transmission medium via an isolation transformer and a single connector in a physical layer interface device given in the 1st paragraph.

[0127] (3) A physical layer interface device, wherein the 2nd transmitter of the above contains a programmable transmission voltage amplifier further in a physical layer interface device given in the 1st paragraph for waveform generating.

[0128] (4) A physical layer interface device, wherein the 2nd receiver of the above includes further the adaptive equalization circuit and baseline wandering correcting circuit which were integrated in a physical layer interface device given in the 1st paragraph.

[0129] (5) A physical layer interface device, wherein the 2nd receiver of the above and the 2nd transmitter of the above include further the synthetic rise time control facility for decreasing an electromagnetic interference so that an external capacitor may be made unnecessary in a physical layer interface device given in the 1st paragraph.

[0130] (6) A physical layer interface device including further the automatic negotiation circuit for performing auto select of half a/full-duplex operation in a physical layer interface device given in the 1st paragraph.

[0131] (7) A physical layer interface device including further the automatic correcting circuit for giving the immunity to receiving pair line reversal in the 1st operational mode of the above in a physical layer interface device given in the 1st paragraph.

[0132] (8) A physical layer interface device by which the phase locked loop (PLL) using the suitable single crocking device even for which of the 1st, 2nd, 3rd, and 4th operational modes of the above being further included in a physical layer interface device given in the 1st paragraph.

[0133] (9) In a physical layer interface device given in the 1st paragraph, A physical layer interface device, wherein the 1st receiver of the above includes further the smart squelch function to only pass ingress data when a pulse sequence with it is received. [ingress entry-of-data amplitude larger than the minimum signal threshold level and and] [specific]

[0134] (10) A recycle delay line is included in a physical layer interface device given in the 1st paragraph, A physical layer interface device including further the analog phase locked loop (PLL) circuit which can operate so that a current source may be gradually

made one using the signal from this recycle delay line.

[0135] (11) A physical layer interface device including further the automatic gain control circuit for giving baseband wandering correction and the offset for the loss of signal strength in a physical layer interface device given in the 1st paragraph.

[0136] (12) In the physical layer interface device given in the 11th paragraph, the above-mentioned automatic gain control circuit contains two peak detectors, A physical layer interface device being able to operate so that the above-mentioned baseline wandering correction may be given, when the above-mentioned automatic gain control circuit makes the minimum the difference between the two above-mentioned peak detectors.

[0137] (13) In the physical layer interface device given in the 1st paragraph, the adaptive equalization circuit and the analog CMOS circuit are included further, A physical layer interface device, wherein the high-frequency enhancement in the above-mentioned adaptive equalization circuit is given as a function of the middle range frequency circuit in the above-mentioned analog CMOS circuit.

[0138] (14) In the physical layer interface device given in the 13th paragraph, the phase locked loop (PLL) is included further, A physical layer interface device generating by setting up the above-mentioned PLL double the transformer conductor to whom bias of the damping time constant for the above-mentioned adaptive equalization circuit was carried out with the capacitor by which the ratio arrangement was carried out appropriately.

[0139] (15) A physical layer interface device including further the digital phase lock loop (DPLL) circuit which can operate in a physical layer interface device given in the 1st paragraph so that two or more DPLL working speeds may be given using single input frequency.

[0140] (16) A physical layer interface device characterized by including the 1st way and /6.25 dividing stage which pass along the 1st delay line in a PLL feedback loop in order that the above-mentioned DPLL circuit may give one of two or more of the above-mentioned DPLL working speeds in a physical layer interface device given in the 15th paragraph.

[0141] (17) A physical layer interface device containing the 2nd way and /2 dividing stage which pass along the 2nd delay line in the above-mentioned PLL feedback loop for giving other things of two or more above-mentioned DPLL working speeds in a physical layer interface device given in the 16th paragraph.

[0142] (18) A physical layer interface device including further the control logic circuit for choosing one of the 1st and 2nd ways of the above in a physical layer interface device given in the 17th paragraph.

[0143] (19) In a physical layer interface device given in the 1st paragraph, the cascade gate voltage within a control feedback loop is controlled to give a high precision reference current to this physical layer interface device, A physical layer interface device including further the reference current circuit it is made to decrease in number without the influence of the limited input impedance in a current mirror sacrificing voltage control capability by that cause.

[0144] (20) It is for synchronizing with the above-mentioned input signal the equalizing circuit which can operate, and the above-mentioned physical layer impedance device in a physical layer interface device given in the 1st paragraph, so that the loss of the received signal by the 2nd transmitter of the above may be compensated, The phase locked loop (PLL) circuit which has a voltage control output portion which gives bias voltage as an output, A physical layer interface device including further the resistance / capacitor circuit network circuit for determining the amount of equalization as a function of frequency according to the above-mentioned bias voltage output from the above-mentioned PLL.

[0145] (21) In the method of being in the differential line receiver which can operate so that a differential signal input may be accepted, and giving signal level control, The step which gives the internal resistance machine network partial pressure network which can operate so that voltage swing of the above-mentioned differential signal input may be decreased, Can operate so that the loss which reinforced the above-mentioned differential signal input according to the 1st return signal, and was produced at the time of transmission may be compensated, and. The step which gives an amplifier means by which it can operate so that wandering of the baseline of the above-mentioned differential signal input may be compensated according to the 2nd return signal and a differential signal output may be generated, The step which measures the high level of the above-mentioned differential signal input using the 1st peak voltage detector, The step which measures the low level of the above-mentioned differential signal input using the 2nd peak voltage detector, the above of the above-mentioned differential signal input -- a high level and the above -- with the step which generates a baseline signal according to a low level. The step which determines the 1st regulation value in order to compensate wandering of a baseline, The step which adjusts the 1st return signal of the above according to the regulation value of the above 1st, the step which determines the 2nd regulation value in order to compensate the above-mentioned loss produced at the time of transmission, and the step which adjusts the 2nd return signal of the above according to the regulation value of the above 2nd, A method possessing the step which gives the above-mentioned differential signal output to a compensator since the data out signal adjusted to wandering of a baseline and the above-mentioned loss produced at the time of transmission is generated.

[0146] (22) In a method given in the 21st paragraph, the above-mentioned step which determines the 1st regulation value, A method by which the step which filters the above-mentioned baseline signal, and the step compare the baseline signal filtered [above-mentioned] to the 1st reference voltage, and it was made to generate the 1st control

signal of the above being included further.

[0147] (23) In a method given in the 21st paragraph, the above-mentioned step which generates the 2nd control signal, A method by which the step which generates an output voltage signal by being between [one pair of] resistance and dropping the above-mentioned quantity and low of the above-mentioned differential signal input, and the step which compares the above-mentioned output voltage signal to the 2nd reference voltage, and generates the 2nd control signal being included further.

[0148] (24) In the device which is in a physical layer interface device and gives a signal control, Voltage swing of a differential signal input so that it may decrease The voltage voltage divider circuit which can operate, So that the above-mentioned differential signal input may be adjusted so that wandering of a baseline and the loss of signal strength may be compensated according to the return signal from a feedback circuit, and this may generate a differential signal output The adjustable amplifier circuit which can operate, A device characterized by the above-mentioned feedback circuit which can operate, and providing the compensator which can operate so that a data out signal may be generated according to the above-mentioned differential signal output so that wandering of the above-mentioned baseline and the loss of the above-mentioned signal strength may be measured and the above-mentioned return signal may be generated according to it.

[0149] (25) In a device given in the 24th paragraph the above-mentioned feedback circuit, So that a high level of the above-mentioned differential signal output from the above-mentioned adjustable amplifier circuit may be measured The 1st peak voltage detector that can operate, So that the low of the above-mentioned differential signal output from the above-mentioned adjustable amplifier circuit may be measured The 2nd peak voltage detector that can operate, A device possessing the circuit which determines the quantity of wandering of a baseline according to the middle value between the above-mentioned high level of the above-mentioned differential signal output, and the above-mentioned low, and the circuit which determines the quantity of signal loss by measuring the above-mentioned differential signal output to reference voltage.

[0150] (26) In the device which is in a physical layer interface device and gives a signal control, Are a voltage voltage divider circuit network and at least one adjustable gain amplifier, and each generates the differential signal output reinforced by reinforcing the specific portion of a differential signal input according to specification frequency spectrum and a related return signal, So that it may be reinforced in the quantity from which the above-mentioned differential signal input of each above-mentioned specification frequency spectrum differed by it At least one adjustable gain amplifier which can operate, it is at least one equalizer means -- each -- the above -- one to which one adjustable gain amplifier related, even if small, [have and] So that the differential signal output by which compensated the differential signal output reinforced [above-mentioned] for line loss, and equalization was carried out by that cause may be generated At least one equalizer means by which it can operate, A device providing the feedback circuit which can operate so that the differential signal output by which equalization was carried out [above-mentioned] may be added, and the adding means

which generates one pair of last differential signal outputs by that cause, wandering of a baseline, and the loss of signal strength may be measured and a return signal may be generated according to it.

[0151] (27) In a device given in the 26th paragraph the above-mentioned feedback circuit, The 1st peak voltage detector means that determines wandering of the baseline of the above-mentioned differential signal output, and adjusts the above-mentioned related return signal according to it, A device including the 2nd peak voltage detector means that determines the signal strength of the above-mentioned differential signal output, and adjusts the above-mentioned related return signal according to it.

[0152] (28) in a device given in the 26th paragraph -- the above -- one adjustable gain amplifier, even if small, So that a constant rate of returns which do not give enhancement to the above-mentioned related part of the above-mentioned differential signal input may be given The 1st thing of three adjustable gain amplifiers that can operate, A device characterized by the 3rd thing of the three above-mentioned adjustable gain amplifiers that can operate, and the thing, ** and others, so that a feedback amount may be given based on the output of the above-mentioned feedback circuit and a feedback amount may be given based on the square of the 2nd thing of the three above-mentioned adjustable gain amplifiers that can operate, and the output of the above-mentioned feedback circuit.

[0153] (29) In the method of being in a physical layer interface device and controlling the damping time constant of an adaptive equalization circuit, The step which generates bias voltage from the voltage controlled oscillator portion of the phase locked loop of the above-mentioned physical layer interface device, A method possessing the step which uses adjustable MOSFET in order to give resistance to the above-mentioned adaptive equalization circuit, and the step which sets up the above-mentioned adjustable MOSFET using the above-mentioned bias voltage.

[0154] (30) Single chip double function 10BASE-T / 100BASE-X physical layer interface device compatible with real 5V part part (PHY) are given. This PHY includes the media non-depending interface (MII), and connects it to a non-covering twisted pair cable via an isolation transformer and RJ45 single connector. This PHY includes the built-in automatic negotiation circuit in which the auto select of all the /half-duplex 10BASE-T and 100BASE-TX is made to perform, and an automatic polarity correcting circuit secures the immunity performance to receiving pair reversal in 10BASE-T operational mode in the case of that auto select. Although this PHY contains including the internal PLL circuit, 20 MHz clocks, i.e., a crystal, with this single, it suits both of the operational modes. This PHY contains low electric power and electric power downward (power down) mode. The 10BASE-T portion of this PHY contains the on-board transmission waveform molding part. The 100BASE-X portion of this PHY includes the synthetic rise time control circuit for decreasing an electromagnetic interference (EMI). This PHY includes the adaptive equalization circuit and baseline wandering correction (DC recovery) circuit for the programmable transmission voltage amplifier for generating 100BASE-X-MLT-3 waveform, and a 100BASE-X receiver which were integrated.

[Claim(s)]

[Claim 1] A physical layer interface device comprising:
The 1st receiver for the 1st operational mode.
The 2nd receiver for the 2nd operational mode.
The 1st transmitter for the 3rd operational mode.
A control circuit which determines operational mode as the 2nd transmitter for the 4th operational mode, chooses a suitable receiver from the 1st and 2nd receivers of the above, and/or chooses a suitable transmitter from the 1st and 2nd transmitters of the above.

[Claim 2] A method characterized by comprising the following of being in a differential line receiver which can operate so that a differential signal input may be accepted, and giving signal level control.
A step which gives an internal resistance voltage divider line network which can operate so that voltage swing of the above-mentioned differential signal input may be decreased.
A step which gives an amplifier means by which it can operate so that it can operate so that a loss which reinforced the above-mentioned differential signal input according to the 1st return signal, and was produced at the time of transmission may be compensated, and wandering of a baseline of the above-mentioned differential signal input may be compensated according to the 2nd return signal and a differential signal output may be generated.
A step which measures a high level of the above-mentioned differential signal input using the 1st peak voltage detector.
A step which measures a low level of the above-mentioned differential signal input using the 2nd peak voltage detector.
the above of the above-mentioned differential signal input -- a high level and the above -- a step which generates a baseline signal according to a low level.
A step which determines the 1st regulation value in order to compensate wandering of a baseline.
A step which adjusts the 1st return signal of the above according to a regulation value of the above 1st, A step which determines the 2nd regulation value in order to compensate the above-mentioned loss produced at the time of transmission, A step which gives the above-mentioned differential signal output to a compensator since a data out signal adjusted to a step which adjusts the 2nd return signal of the above according to a regulation value of the above 2nd, and wandering of a baseline and the above-mentioned loss produced at the time of transmission is generated.

TABLE 1

CSPEED	CDUPLEX	10Mbps HDX	10Mbps FDX	100Mbps HDX	100Mbps FDX
1	1	Ye	Yee	Yes	Yes
1	0	Yes	Yes	Yes	No
0	1	Yes	Yes	No	No
0	0	Yes	No	No	No

TABLE 2

Bit	Name	Function
15	RESET	PHY Reset: Writing a one to this bit will cause the PHY to be reset and all registers except GEN_ctl to be reset to their default values. RESET is self-clearing - it will return a value of one when read until the internal reset is complete (which will take no longer than 500ms). Writing a zero to RESET to zero (default) has no effect. This bit is self-clearing and defaults to zero. NOTE: This operation may interrupt data communications.
14	LOOPBK	Loopback: This bit enables/disables internal loopback within the PHY device. When LOOPBK is set to one (default), data is internally wrapped within the PHY and does not appear on the network. When LOOPBK is cleared to zero, data is transmitted to and received from the network. Whilst the PHY is in loopback all network lines are placed in a non-contentious state. The value read as the LOOPBK bit is the logical OR of the register bit and the (active low) CLOOPBK# pin (external enable).
13	SPEED	Speed Select: Link speed can be selected via either the Auto-negotiation process, or manual speed selection. The default value of this bit is one. Manual speed selection is available when Auto-negotiation has been disabled. The speed is determined either by the value of this bit (when AUTONEG is zero) or the value of the CSPEED pin (when AUTONEG is one and the CAUTONEG pin is low). When Auto-negotiation is disabled, setting SPEED to one (default) configures the PHY for 100Mbps operation, and clearing SPEED to zero configures PHY for 10Mbps operation. The value read from the SPEED bit reflects the currently selected speed mode, whatever the source of the configuration may be (i.e., this bit, the CSPEED pin or the result of a negotiation).
12	AUTONEG	Auto-negotiation Enable: This bit enables/disables the Auto-negotiation process. When AUTONEG is zero, the link shall be configured via the DUPLEX and SPEED bits, and the PHY will implement the appropriate link integrity test. When AUTONEG is set to one (default), Auto-negotiation is enabled and the PHY will engage in the Auto-negotiation process when a LINk FAIL condition is detected or the AUTORSRT bit is set. The link should not be treated as valid until the AUTOCMPLT bit and LINK bit both become set to one as Auto-negotiation may complete having found no common line configuration. The value read as the AUTONEG bit is the logical OR of the register bit and the (active low) CAUTONEG pin (external disable).
11	PDOWN	Power-down: When PDOWN is set to one, the PHY is placed in a low power consumption state. The time required for the PHY to power up after this bit is cleared can vary considerably, primarily based on whether a crystal or crystal oscillator is connected to XTAL1/XTAL2. It is good practice to set RESET after this time to ensure the PHY is in a valid state (this is unlikely to be necessary when a crystal oscillator is used). The default value of PDOWN is zero. The value read as the PDOWN bit is the logical OR of the register bit and the (active low) CPWRDOWN# pin (external enable).
10	ISOLATE	Isolate: The function of ISOLATE is differs depending on whether the PHY is in Repeater mode or Node mode (determined by the REPEATER bit in TLPHY_ctl). In Node mode, when ISOLATE is set to one (default), the PHY will electrically isolate its data paths from the MII. In this state is will not respond to MTXD0-3, MTXEN, and MTXER inputs, and will present a high impedance on its MTCLK, MRCLK, MRXDV, MRXER, MRXD0-3 and MCOL outputs. It will however still respond to management frames on MDIO and MDCLK. In Repeater mode, when ISOLATE is set to one (default) the PHY will present a high impedance on its MRCLK, MRXDV, MRXER and MRXD0-3 outputs only. The value read as the ISOLATE bit is the logical AND of the register bit and the (active low) CISOLATE# pin (external disable).
9	AUTORSRT	Restart Auto-negotiation: If Auto-negotiation has been enabled by setting AUTONEG to one, the Auto-negotiation process can be restarted by setting AUTORSRT to a one. AUTORSRT is self clearing, and the PHY shall return a value of one in this bit until Auto-negotiation FLP data burst transmission has been initiated. When AUTONEG is cleared to zero, AUTORSRT will read as zero. The default value of AUTORSRT is zero.
8	DUPLEX	Duplex Mode: Duplex mode can be selected via either the Auto-negotiation process, or manual duplex selection. Manual duplex selection is available when Auto-negotiation has been disabled. The duplex configuration is determined either by the value of this bit (when AUTONEG is zero) or the value of CDUPLEX pin (when AUTONEG is one and the CAUTONEG pin is low). When Auto-negotation is disabled, setting DUPLEX to one configures the PHY

TABLE 2-continued

Bit	Name	Function
		for full duplex operation, and clearing SPEED to zero (default) configures the PHY for half duplex operation. The value read from the DUPLEX bit reflects the curently selected duplex mode, whatever the source of the configuration may be (i.e., this bit, the CDUPLEX pin or the result of a negotation).
7	COLTEST	Collision Test Mode: When COLTEST is set to one and LOOPBK is set to one, the PHY will assert the collision detect signal MCOL whenever transmit enable MTXEN is asserted. The default value of COLTEST is zero.
6 thru 0		Reserved: Read and write as zero

TABLE 3

Bit	Name	Function
15	0	100BASE-T4 Ability: Not supported.
14	1	100BASE-TX Full-Duplex Ability: Supported by this PHY.
13	1	100BASE-TX Half-Duplex Ability: Supported by this PHY.
12	1	10BASE-T Full-Duplex Ability: Supported by this PHY.
11	1	10BASE-T Half-Duplex Ability: Supported by this PHY.
10 thru 7		Reserved: Read and write as zero
6	1	MF Preamble Suppression: This PHY will accept management frames with preamble suppressed. Management frames sent over MDIO do not need to be preceded by the preamble pattern of 32 one's.
5	AUTOCMPLT	Auto-Configuration Complete: When AUTOCMPLT is read as one, it indicates that the Auto-negotiation process has completed and the values of registers AN_adv, AN_lpa, AN_exp and AN_np are valid If Auto-negotiation is in progress, or has been restarted and AUTORSRT is still set to one, or has been disabled by clearing AUTONEG to zero, the AUTOCMPLT bit will read as zero.
4	RFAULT	Remote Fault: The RFAULT bit will be set to one during Auto-negotiation if an error in the protocol is detected and negotiation is restarted. If the negotiation involved the exchange of multiple Next Pages this bit will indicate that the first of those pages needs to be reloaded into AN_np due to the restart. RFAULT is latched (held) as one until the register is read. The default value of RFAULT is zero.
3	1	Auto-negotiation Ability: This PHY supports Auto-negotiation.
2	LINK	Link Status: In general, when LINK is set to one, the PHY is reporting a good link is available to the link partner for exchange of data. The value of LINK is latched (held) until the register is read. The default value of LINK is one. In 10BASE-T mode LINK is set to one when the PHY has determined that a valid 10BASE-T link is established. When read as a zero it indicates that the link is not valid. The PHY implements the standard 10BASE-T link integrity test state machine. Linkpulses are expected to be seen every 8–24ms to maintain a good link. If no linkpulses are seen for over 100ms the link invalid state is entered, and this bit is cleared. If AUTONEG is not set then the bit will be set again after seven consecutive, correctly timed linkpulses are received. In 100BASE-X mode the LINK bit is set once the descrambler has locked onto the incoming data stream, and has remained locked for a minimum of 330μs. If AUTONEG is set then the link becoming invalid causes the auto-negotiation process to restart.
1	JABBER	Jabber detect: The Jabber function is not specified for 100BASE-X PHYs so JABBER will always read as zero (default) when the PHY is operating in its 100Mbps mode. When JABBER is read as one it indicates a 10BASE-T jabber condition has been detected. JABBER is latched (held) as one until the register is read. The jabber condition occurs when a single packet transmission exceeds 20ms (note this cannot happen through normal TLAN operation). In the jabber condition all transmit requests will be

TABLE 3-continued

Bit	Name	Function
		ignored, the MCOL pin will be asserted high and collision detection will be disabled as will the internal loopback of transmit data (when in half duplex mode). The jabber condition will persist for 576m–628ms after the de-assertion of MTXEN before packet transmission may recommence.
0	1	Extended Capability: This PHY implements an extended register set.

[Table 4]

TABLE 4

Bit	Name	Function
15	NP	Auto-negotiation Next Page: When NP is set to one the Auto-negotiation process will indicate to the Link Partner that the PHY wishes to exchange Next Pages. The capability of the Link Partner to exchange Next Pages can be determined by the value of the LPNPABLE bit in register AN_exp. If the Link Partner is capable of Next Page exchange and has also requested an exchange by setting the LPNP bit to one in the AN_lpa register, then the Auto-negotiation process will wait until the Next Page is written to the AN_np register, and the Link Partner has also had its Next Page loaded. The Link Partner's Next Page will then be received into the AN_lpa register. A consequence of this process is that the PHY will fail to complete Auto-negotiation if for some reason the PHY and its Link Partner agree to exchange Next Pages, but the Link Partner never sends its Next Page. It is advised that a software timeout is implemented which will force re-negotiation with NP cleared to zero to escape this deadlock situation. The default value of NP is zero.
14		Acknowledge: Reserved for internal use of the Auto-negotiation process. Write as zero, read as Don't Care.
13	RF	Remote Fault: When RF is set to one the PHY will indicate a Remote Fault condition to its Link Partner. The type of fault as well as the criteria and method of fault detection is PHY specific. The default value of RF is zero.
12 thru 9	Technology Ability Field	Auto-negotiation Advertised Technology Ability: This 8-bit value is sent to the Link-Partner to indicate the abilities of the TLAN PHY. Unsupported ab/ilities cannot be advertised, which for this PHY means bits 12 thru 9 are read-only and always read as zero. The default value of the Technology Ability Field is to advertise all available capabilities (0000.1111).
8		100BASE-TX Full duplex: Set to one to advertise availability to the Link Partner.
7		100BASE-TX Half duplex: Set to one to advertise availability to the Link Partner.
6		10BASE-T Full duplex: Set to one to advertise to availability the Link Partner.
5		10BASE-T Half duplex: Set to one to advertise to availability the Link Partner.
4 thru 0	Selector Field	Auto-negotiation Selector Field Code: This field has a default value of 0001, meaning the PHY only supports IEEE 802.3 format link code words.

TABLE 5

Bit	Name	Function
15	LPNP	Link Partner Next Page: When LPNP is set to one the Link Partner is indicating that it wishes to exchange a Next Page. See the description of NP in register AN_adv for more information on Next Page exchange.
14		Acknowledge: Reserved for internal use of the Auto-negotiation process. Write as zero, read as Don't Care.
13	LPRF	Link Partner Remote Fault: When this bit is set to a one the Link Partner is reporting a remote fault condition.
12 thru 10	Link Partner Technology Ability Field	Link Partner Technology Ability Field: This 8-bit value specifies which capabilities the Link Partner PHY implements. Bits 12 thru 10 are reserved for future IEEE defined abilities and cannot be defined at this time (except that this PHY does not support them).
9		100BASE-T4: Set to one if supported by the Link Partner.
8		100BASE-TX Full duplex: Set to one if supported by the Link Partner.
7		100BASE-TX Half duplex: Set to one if supported by the Link Partner.
6		10BASE-T Full duplex: Set to one if supported by the Link Partner.
5		10BASE-T Half duplex: Set to one if supported by the Link Partner.
4 thru 0	Link-Partner Selector Field	Link Partner Selector Field: This 5-bit value encodes the format of this register. The PHY only supports IEEE 802.3 format fields (as detailed in bits 12 thru 5 above), code 00001. (The only other currently specified IEEE value is 00010, for IEEE 802.9a multimedia frames).

TABLE 6

15	LPNP	Link Partner Next Page: When LPNP is set to one the Link Partner is indicating that it wishes to exchange a further Next Page. See the description of NP in register AN_adv for more information on Next Page exchange.
14		Acknowledge: Reserved for internal use of the Auto-negotiation process. Read as Don't Care.
13	LPMP = 1	Link Partner Message Page: When LPMP is set to one, register AN_lpa contains a Message Page.
12		Acknowledge 2: Reserved for internal use of the Auto-negotiation process. Read as Don't Care.
11		Toggle: Reserved for internal use of the Auto-negotiation process. Read as Don't Care.
10 thru 0	Message Code Field	Message Code: 11-bit Message Code. See Message Code Field Values for descriptions of the currently defined IEEE Message Codes.

TABLE 7

15	LPNP	Link Partner Next Page: When LPNP is set to one the Link Partner is indicating that it wishes to exchange a further Next Page. See the description of NP in register AN_adv for more information on Next Page exchange.
14		Acknowledge: Reserved for internal use of the Auto-negotiation process. Read as Don't Care.
13	LPMP = 0	Link Partner Message Page: When LPMP is cleared to zero, register AN_lpa contains an Unformatted Page.
12		Acknowledge 2: Reserved for internal use of the Auto-negotiation process. Read as Don't Care.
11		Toggle: Reserved for internal use of the Auto-negotiation process. Read as Don't Care.
10 thru 0	Unformatted Code Field	Unformatted Code: 11-bit user code. The format of this code is determined by the preceding Message Code. See Message Code Field Values.

[Table 8]

TABLE 8

Message Code #	Bit 10 thru Bit 0	Message Code Description
0	00000000000	Reserved for future Auto-negotiation use
1	00000000001	Null Message: The Null Message code shall be transmitted during Next Page exchange when the local devjce has no further messages to transmit and the Link Partner is still transmitting valid Next Pages.
2	00000000010	Technology Ability Extension Code 1 (one UP with Technology Ability Field follows): This Message Code is reserved for future expansion of the Technology Ability Field and indicates that a defined user code with a specific Technology Ability Field encoding follows.
3	00000000011	Technology Ability Extension Code 2 (two UPs with Technology Ability; Fields follow): This Message Code is reserved for future expansion of the Technology Ability Field and indicates that two defined user codes with specific Technology Ability Field encoding follow.
4	00000000100	Remote Fault Number Code (one UP with Binary coded Remote Fault follows): This Message Code shall be followed by a single user code whose encoding specified the type of fault that has occurred. The following user codes are defined: 0 RF Test: Used to test Remote Fault operation. 1 Link Loss 2 Jabber 3 Parallel Detection Fault: Sent to identify when PDFAULT is set.
5	00000000101	Organizationally Unique Identifier Tagged Message: The OUI Tagged Message shall consist of a singled message code of 0000.0000.0101 followed by 4 user codes defined below. The numbers indicate where each bit of the 24-bit OUI should be stored in the 11-bit user code. Bits 8-0 of the 3rd user code and the fourth and final user code shall contain a user defined user code value that is specific to the OUI transmitted.

	Bit 10										Bit 0
	User Code Encoding of Organizationally Unique Identifier										
1st	23	22	21	20	19	18	17	16	15	14	13
2nd	12	11	10	9	8	7	6	5	4	3	2
3rd	1	0	User Defined User Code Specific to OUI								
4th	User Defined User Code Specific to OUI										

6	00000000110	PHY Identifier Tag Code The PHY ID tag code message shall consist of a single message code of 0000.0000.0110 followed by 4 user codes defined below. The numbers indicate where each bit of the 32-bit PHY ID (stored in GEN_id_hi register 0x2:15-0 and GEN_id_lo register 0x3:15-0) should be stored in the 11-bit user code. Bit 0 of the 3rd user code and the fourth and final user code shall contain a user defined user code value that is specific to the PHY ID transmitted.

	Bit 10										Bit 0
	User Code Encoding of PHY ID										
1st	0x2 15	0x2 14	0x2 13	0x2 12	0x2 11	0x2 10	0x2 9	0x2 8	0x2 7	0x2 6	0x2 5
2nd	0x2 4	0x2 3	0x2 2	0x2 1	0x2 0	0x3 15	0x3 14	0x3 13	0x3 12	0x3 11	0x3 10
3rd	0x3 9	0x3 8	0x3 7	0x3 6	0x3 5	0x3 4	0x3 3	0x3 2	0x3 1	0x3 0	UD UC
4th	User Defined User Code Specific to PHY ID										

2047	11111111111	Reserved for future Auto-negotiation use

TABLE 9

Bit	Name	Function
15 thru 5		Reserved: Read and write as zero.
4	PDFAULT	Parallel Detection Fault: The PDFAULT bit is set to one during Auto-negotiation if the PHY detects a valid 10BASE-T or 100BASE-TX link which then fails within 500–1000ms, or if both the 10BASE-T and 100BASE-TX link monitors report a good link. PDFAULT is latched (held) until this register is read, when it is cleared to zero (default).
3	LPNPABLE	Link-Partner Next Page Able: When LPNPABLE is set to one, the Link-Partner is indicating that it implements the Auto-negotiation Next Page ability. The default value of LPNPABLE is zero.
2	1	Next Page Able: This PHY supports Auto-negotiation Next Page exchange.
1	PAGERX	Page Received: The PAGERX bit is set to one when a new Link Code Word has been received and stored in the AN_lpa register. PAGERX is latched (held) until this register is read, when it is cleared to zero (default).
0	LPANABLE	Link-Partner Auto-Negotiation Able: When LPANABLE is set to one the PHY has received Link Code Word(s) from the Link Partner during Auto-negotiation. The value of LPANABLE is retained after Auto-negotiation completes, and will be re-evaluated only during a subsequent re-negotiation (whether caused by a LINK FAIL condition or a forced restart) or PHY reset. The default value of LPANABLE is zero.

TABLE 10

Bit	Name	Function
15	NP	Next Page: When a Next Page with NP set to one is transmitted, the I Partner is informed that yet another Next Page is to be transmitted. Message Code Field Values. The default value of NP is zero.
14		Acknowledge: Reserved for internal use of the Auto-negotiation pro Write as zero, read as Don't Care.
13	MP	Message Page: When MP is set to one, AN_np contains a Message code field. When MP is cleared to zero, AN_np contains an Unform Page code field. See Message Code Field Values. The default value of is zero.
12		Acknowledge 2: Reserved for internal use of the Auto-negotiation pro Write as zero, read as Don't Care.
11		Toggle: Reserved for internal use of the Auto-negotiation process. Wri zero, read as Don't Care.
10 thru 0	Message/ Unformatted Code Field	Message or Unformatted Code Field: See Message Code Field Values. T default value of the code field is 000.0000.0001, the Null Message code.

TABLE 11

Bit	Name	Function
15	IGLINK	Ignore Link: When IGLINK is cleared to zero (default), the 10BASE-T P expects to receive link pulses from the link partner (hub, switch, etc.) and clear the LINK bit in the GEN_sts register to zero if they are not pres When IGLINK is set to one the internal link integrity test state machin forced to stay in the LINK GOOD state even when no link pulses are b received, and also causes the LINK bit to stay set to one.
14	SWAPOL	Swap Polarity: When enabled via the MANCONF bit, writing a one SWAPOL will cause the PHY to use the reverse of the IEEE 802.3 standa polarity for the ARCVP/ARCVN 10BASE-T receiver input pair. This is us to compensate for a cable in which the receive pair have been incorrect wired. When SWAPOL is set to zero or MANCONF is set to zero, the PHY w attempt to automatically sense and correct for an inverted 10BASE-T recei pair. The default value of SWAPOL is zero.
13	MANCONF	Manual Configuration: Writing a one to MANCONF enables manu configuration of the PHY. The SWAPOL bit has no effect unless this bit set. The default value of MANCONF is zero.
12	SQEEN	SQE (Signal Quality Error or "Heartbeat") Enable: When SQEEN is set one the 10BASE-T PHY (when selected) will perform the SQE test function the end of packet transmission. The default value of SQEEN is zero. The Signal Quality Error test provides an internal simulated collision test collision detect circuit integrity after a transmission. In 10BASE-T mo the SQE test asserts MCOL between 600ns–1600ns after the last posit edge of a frame is transmitted, with the collision event lasting for betwe 500ns–1500ns.
11	MTEST	Manufacturing Test: When MTEST is set to one the PHY is placed i manufacturing test mode. Manufacturing test mode is reserved for Te Instruments Manufacturing test only. The default value of MTEST is ze Operation of the PHY and MII registers is undefined when this bit is set.
10	FIBRE	100BASE-FX Mode: When FIBRE is set to one the PHY will disable cipher stream scrambler and descrambler. The default value of FIBRE zero.
9	FEFEN	Far End Fault Indication Enable: When both FEFEN and FIBRE are se one the PHY will transmit the Far End Fault Indication symbol stre (consisting of 84 one's and 1 zero) whenever the 100BASE-FX signal detec de-asserted. Also at this time, the FEFI bit in TLPHY_sts will become se one. The FEFI system is specified for use in 100BASE-FX Fibre applicati only. The default value of FEFEN is zero.
8	NOENDEC	No Encode/Decode: When NOENDEC is set to one the 100BASE-X PHY w bypass its 4B5B encoder and decoder. Instead it will take the 5-bit co presented on MTXD0-3 and MTXER (msb) as transmit data, and w present the received 5B code groups on MRXD0-3 and MRXER (msb). T default value of NOENDEC is zero. The value read as the NOENDEC bit is the logical OR of the register and the (active low) CPASS5B# pin (external enable).
7	NOALIGN	No Symbol Alignment: When NOALIGN is set to one the 100BASE-X recei symbol alignment block is bypassed and the 5-bit descrambled recei symbols are passed directly to the 5B4B decoder.
6	DUPONLY	Duplex LED: When DUPONLY is set to one the LDUPCOL# LED driv will only indicate the duplex mode the PHY is operating in, and will r indicate network collisions. The default value of DUPONLY is zero.
5	REPEATER	Repeater Mode Enable: When REPEATER is set to one the PHY will assert MCRS in response to transmit activity. Also, the ISOLATE bit in GEN_ctl register will only tristate the MRCLK, MRXD0-3, MRXDV a MRXER pins. The default value of REPEATER is zero.
4	RXRESET	100BASE-X Receive Reset: Writing a one to this self-clearing bit allows t 100BASE-X receive logic (descrambler, aligner and SB4B decoder) to be re without affecting other parts of the PHY. The default value of RXRESET zero.
3	NOLINKP	Disable Linkpulse Transmission: When NOLINKP is set to one a IGLINK is set to one the PHY will not transmit any form of link pulses. 10BASE-T applications the Link Partner will not detect a good link and will not transmit any data, unless it is not implementing the Link Integ Test (e.g., a TLAN PHY with IGLINK set to one). Auto-negotiation should disabled by clearing AUTOENB to zero when NOLINKP is set as no Au negotiation fast link pulses will be transmitted to the Link Partr NOLINKP has no effect on the PHY if IGLINK is cleared to zero. default value of NOLINKP is zero. This mode of operation is provided application test purposes.
2	NFEW	Not Far End Wrap: This bit only has meaning when the LOOPBK bit of t GEN_ctl is set to one. Writing a one to NFEW will cause the PHY to wr the MTXD input data to the MRXD output just after the MII interfac Writing a zero to NFEW will cause the PMI to wrap the TX data to the just before the network transceiver interface (either 10BASE-T or 100BAS

TABLE 11-continued

Bit	Name	Function
		TX). When NFEW is set to one preamble will be wrapped witho degradation (in normal operation the PHY may lose some preamble b during initial clock recovery synchronization). The default value of NFEW zero.
1	INTEN	Interrupt Enable: Writing a one to INTEN allows the PHY to genera interrupts on the MII when the MINT bit is set to one. Writing a zero INTEN will prevent the PHY from generating any MII interrupts. INT does not disable test interrupts. The default value of INTEN is zero.
0	TINT	Test Interrupt: When TINT is set to one the PHY will generate interrupts the MII, irrespective of the value of the MINT and INTEN bits. TINT is be used for diagnostic test of the MII interrupt function. The default value TINT is zero.

TABLE 12

Bit	Name	Function
15	MINT	MII Interrupt. This bit indicates an MII interrupt condition. The MII interrupt request will be activated and latched (held) until this register is read. Writing to this bit has no effect. MINT is set to one when: • PHOK changes state. • LINK changes state, or is different from either the last read value or the current state of the link. • SYNCLOSS becomes set to a one. • FEFI becomes set to one. • JABBER changes state. • RFAULT becomes set to a one. • PAGERX becomes set to a one. • AUTOCMPLT changes state. These interrupt sources are only active when MANCONF in TLPHY_ctl is set to one, and set MINT to one when: • SIGDET changes state. • POLOK changes state.
14	PHOK	Power High O.K.: When PHOK becomes set to one it indicates that the internal crystal oscillator circuit has begun to oscillate (and performed around 75 cycles). PHY sourced clocks (MRCLK and MTCLK) are not valid until at least the time that this bit is asserted. If a crystal is connected to XTAL1/XTAL2 rather than a crystal oscillator then the clocks may take up to 50ms to become stable, and the PHY will require the RESET bit to be set to ensure it is in a valid state. When PHOK is zero the PHY is not in a fully operational state.
13	POLOK	Polarity O.K: When POLOK is set to one (default) the 10BASE-T PHY is receiving valid (non-inverted) link pulses. If POLOK becomes cleared to zero, it indicates that a sequence of 7 consecutive inverted link pulses have been detected. POLOK is reset to one whenever a normal link pulse is received.
12	SIGDET	100BASE-X Signal Detect: When SIGDET is set to one it indicates that the PHY is receiving valid 100BASE-X signaling. If the PHY is operating in fibre mode then this bit reflects the value on the FSDPIFSDN pins otherwise it indicates that the on-chip 100Mbps receiver equalizer has settled.
11	SYNCLOSS	100BASE-TX Receive Descrambler Synchronization Loss: The 100BASE-TX descrambler expects to receive at least 12 consecutive IDLE symbols every 722μs. If these are not seen then SYNCLOSS is set to one, and the descrambler will attempt to re-synchronize itself to the incoming scrambled data stream. The value of SYNCLOSS is latched (held) high until this register is read.

TABLE 12-continued

Bit	Name	Function
10	FEFI	Far End Fault Indication: When enabled via the FEFEN bit in TLPHY_ctl, this bit will be set to one if the FEFI signaling sequence is being transmitted by the link partner. The value of FEFI is latched (held) high until this register is read.
9 thru 0		Reserved: Read and write as zero

[Table 13]

TABLE 13A

Network Interface Pins

Pin	Name	Type	Function
1	ACPLL	an	P.L.L. capacitor: Capacitor required for an internal phase-locked loop. Value T.B.D.
2	ACBLW	an	B.L.W. Capacitor: Capacitor for the Baseline-Wander correction loop. Value T.B.D.
3	ACAGC	an	A.G.C. Capacitor: Capacitor for the Automatic Gain Control loop. Value T.B.D.
4	AVDD	supply	Power: Analog 3.3V supply connection.
5	AVDD		
6	AIREF	an	Analogue Current Reference: An external resistor between this pin and analog ground sets the bias current for internal analogue circuits. Value T.B.D. but currently at 7500 Ohms +/- 1%.
7	AGNDS	supply	Ground: Independent ground connection for the internal device scribe seal. Connect to analog GND.
8	ATXREF	an	100BASE-TX Transmit Reference: An external resistor between this pin and analog ground sets the 100 BASE-TX transmit amplitude. Value T.B.D. but currently at 2500 Ohms +/- 1% for U.T.P.
9	AGND	supply	Ground: Analog Ground connection.
10	AGND		
11	XTAL1	3.3V	Crystal: Connect a 20MHz crystal and capacitor network
12	XTAL2	an	between these pins or drive XTAL1. Alternatively an external crystal oscillator (with a maximum output of 3.3V) may be connected to these pins.
13	AVDD	supply	Power: Analog 3.3V Supply connection.
14	AVDD		
15	ATEST1	an	Analogue Test1: A T.I. analog test pin. Treat this pin as a no-connect (N/C).
16	AGND	supply	Ground: Analog Ground connection.
17	N/C		No connect: Leave this pin unconnected.

Key to Pin Types:
in Input only pin
out Output only pin
t/s Tri-state I/O pin
o/d Open Drain output pin
an Analogue signal pin
supply Power Supply or ground pin

TABLE 13B

External Configuration Pins

Pin	Name	Type	Function
18 19 20	CDEVSEL0 CDEVSEL1 CDEVSEL2	3.3V In	MII Device Select Address bit 0: The value of CDEVSEL0-4 pins are latched into the MII Management Interface on the rising edge of MRST#. This allows a unique address to be assigned to the PHY in applications where multiple PHYs are in use.
21	CREPEATER#	3.3V In	Repeater Mode Enable: This pin is logically OR-ed with the REPEATER bit in the TLPHY_ctl register to enables (active low)/disable repeater mode.

TABLE 13B-continued

External Configuration Pins

Pin	Name	Type	Function
22	CSERTEST#	3.3V In	Reserved for TI Manufacturing Test. Connect to VDD via a pull-up resistor. In serial test mode, auto-negotiation is disabled and selecting 10Mbps mode will cause the PHY to power down.
23	DVDD	supply	Power: Digital 3.3V supply connection.

TABLE 13C

LED Interface Pins

Pin	Name	Type	Function
24	LACTIVITY#	3.3V Out	Activity Indicator: This driver will light an attached LED in response to both receive and transmit activity within the PHY.
25	LDUPCOL#	3.3V Out	Duplex/Collision Indicator: This driver will light an attached LED in response to a network collision when the PHY is in a half-duplex mode of operation. The LED will be lit continuously when the PHY is in a full-duplex mode.
26	DGND	supply	Ground: Digital Ground connection.
27	LLINK#	3.3V Out	Link Status Indicator: This driver will ight an attached LED when the PHY has established a valid link with its partner. If auto-negotiation is enabled the driver will flash the LED during negotiation to indicate that it is attempting to establish a link. This is useful as a negotiation takes a minimum of 3 seconds (considerably longer if Next Page information is also being exchanged) and the user may be tempted to remove the cable if the link light does not come on immediately. The user will also be alerted to a network mis-configuration (where no common ability exists between the two link partners) by a continuously flashing LED.
28	LSPEED #	3.3V Out	Link Speed Indicator: This driver will light an attached LED when the PHY has established a valid 100BASE-X link with its partner.
29	DGND	supply	Ground: Digital Ground connection.

TABLE 13D

External Configuration Pins

Pin	Name	Type	Function
30	CLOOPBK#	In	Loopback Enable: This pin enables (active low)/disables internal loopback within the PHY device and is equivalent to the LOOPBK bit in the GEN_ctl register except that the pin is Active LOW.
31	+5V	supply	Power: Digital 5V supply connection.
32	CPWRDOWN#	In	Power-down Enable: This pin enables (active low)/disables internal loopback within the PHY device and is equivalent to the PDOWN bit in the GEN_ctl register except that the pin is Active LOW.
33	CAUTONEG	In	Auto-negotiation Enable: This pin enables (active high)/disables auto-negotiation within the PHY device when the ANENABLE bit in the GEN_ctl register is set to one. The values of the CSPEED and CDUPLEX pins are latched into the Auto-negotiation logic on the rising edge of CAUTONEG and are used to set the advertised capabilities.
34	CSPEED	I/O	Speed Configuration: When CAUTONEG is low, this pin is logically OR-ed with the SPEED bit the GEN_ctl register to select either 10BASE-T (low) or 100BASE-X (high) mode. After a rising edge on CAUTONEG and a completed negotiation this pin will be driven with the negotiated speed.
35	DVDD	supply	Power: Digital 3.3V supply connection.
36	CDUPLEX	I/O	Duplex Configuration: When CAUTONEG is low, this pin is logically OR-ed with the DUPLEX bit the GEN_ctl register to select either half-duplex (low) or full-duplex (high) mode. After a rising edge on CAUTONEG and a completed negotiation this pin will be driven with the negotiated duplex.

TABLE 13D-continued

External Configuration Pins

Pin	Name	Type	Function
37	CPASS5B#	In	Pass-thru Mode Enable: When CPASS5B# is low, this pin is logically OR-ed with the NOENDEC bit in the TLPHY_ctl register to enable the 5B pass-thru mode. In this mode of operation the normal 4B5B encoding used in 100BASE-X is bypassed. The 5B code group to transmit is taken from MTXD0-3 and MTXER (msb). Receive data is descrambled and aligned and the resulting the 5B code presented on MRXD0-3 and MRXER (msb).
38	CISOLATE#	In	MII Interface Isolate Enable: This pin is logically AND-ed with the ISOLATE bit in the GEN_ctl register to enable (active low)/disable MII Isolate mode. When the PHY is in Node mode, isolating the MII causes the PHY to tristate MTCLK, MRCLK, MRXD0-3, MRXDV, MRXER, MCRS and MCOL and it will not respond to MTXEN. When the PHY is in Repeater mode only MRXCLK, MRXD0-3, MRXDV and MRXER are tristated, hence the CISOLATE# pin acts as an active high Receive Enable function.

TABLE 13E

External Status Pins

Pin	Name	Type	Function
39	SLINK (CDEVSEL3)	I/O	Link Status: When asserted high this pin indicates a good link has been established with the link partner. When auto-negotiation is enabled it also indicates that the CSPEED and CDUPLEX pins are being driven with the negotiated speed and duplex configuration. The value of this pin is latched on the rising edge of MRST# for use as CDEVSEL3, bit 3 of the MII Device Select Address.
40	DGND	supply	Ground: Digital Ground connection.

TABLE 13F

Media Independent Interface Pins

Pin	Name	Type	Function
41	MRST#	In.	MII Reset: Reset signal to the PMD front end (active low).
42	MDIO	I/O	Management Data I/O: Serial management interface to PMD chip. MDIO is synchronous to MDCLK.
43	MDCLK	In	Management Data Clock: Serial management interface to PMD chip.
44	DVDD	supply	Power: Digital 3.3V supply connection.
45	MRXER	Out	Receive Error: Indicates reception of a coding error on received data. MRXER is synchronous to MRCLK.
46	MRXDV	Out	Receive Data Valid: Indicates data on MRXD0-3 is valid. MRXDV is synchronous to MRCLK.
47	MRXD3	Out	Receive Data Bit 3: Nibble Receive data bit 3 from the PHY. Data is synchronous to MRCLK.
48	MRXD2	Out	Receive Data Bit 2: Nibble Receive data bit 2.
49	DGND	supply	Ground: Digital Ground connection.
50	MRXD1	Out	Receive Data Bit 1: Nibble Receive data bit 1.
51	+5V	supply	Power: Digital 5V supply connection.
52	MRXD0	Out	Receive Data Bit 0: Nibble Receive data bit 0.
53	DVDD	supply	Power: Digital 3.3V supply connection.
54	MRCLK	Out	Receive Clock: Receive clock source from the PHY. This clock will be 2.5MHz in 10BASE-T mode, and 25MHz in 100BASE-X mode.
55	MCRS	Out	Carrier Sense: This signal asserts when the PHY initiates a frame reception.
56	MCOL (CDEVSEL4)	I/O	Collision Detect: This signal indicates that the PHY is receiving data whilst also transmitting. This signal will not assert in full-duplex mode.

TABLE 13F-continued

Media Independent Interface Pins

Pin	Name	Type	Function
			The value of this pin is latched on the rising edge of MRST# for use as CDEVSEL4, bit 4 of the MII Device Select Address.
57	MTXER	In	Transmit Error: This signal allows coding errors to be propagated across the MII. MTXER is synchronous to MTCLK.
58	MTXEN	In	Transmit Enable: This signal indicates valid transmit data on MTXD0-3. MFIXEN is synchronous to MTCLK.
59	DGND	supply	Ground: Digital Ground connection.
60	MTXD3	In	Transmit Data Bit 3: Nibble Transmit data bit 3 from the MAC. Data is synchronous to MTCLK.
61	MTXD2	In	Transmit Data Bit 2: Nibble Transmit data bit 2.
62	MTXD1	In	Transmit Data Bit 1: Nibble Transmit data bit 1.
63	MTXD0	In	Transmit Data Bit 0: Nibble Transmit data bit 0.
64	N/C		No connect: Leave this pin unconnected.
65	DVDD	supply	Power: Digital 3.3V supply connection.
66	MTCLK	Out	Transmit Clock: Transmit clock source from the PHY. This clock will be 2.5MHz in 10BASE-T mode, and 25MHz in 100BASE-X mode.

TABLE 13G

JTAG Test Port Pins

Pin	Name	Type	Function
67	JTRST#	In	Test Access Port Reset. Used to reset the test port controller (optional).
68	JTMS	In	Test Mode Select: Used to control the state of the test port controller within the PHY.
69	JTCLK	In	Test Clock: Used to clock state information and test data into and out of the device during operation of the test port.
70	DGND	supply	Ground: Digital Ground connection.
71	JTDO	Out	Test Data Output: Used to serially shift test data and test instructions out of the device during operation of the test port.
72	+5V	supply	Power: Digital 5V supply connection.
73	JTDI	In	Test Data Input: Used to serially shift test data and test instructions into the device during operation of the test port.
74	N/C		No connect: Leave this pin unconnected.
75	DGND	supply	Ground: Digital Ground connection.

TABLE 13H

Serial Test Mode Interface Pins

Pin	Name	Type	Function
76	FXMTN	an	Serial Data Output Pair: Reserved for TI Manufacturing Test.
77	FXMTP	an	Treat as a No Connect.
78	DVDD	supply	Power: Digital 3.3V supply connection.
79	FRCVN	an	Serial Data Input Pair. Reserved for TI Manufacturing Test.
80	FRCVP	an	Treat as a No Connect.
81	DGND	supply	Ground: Digital Ground connection.
82	FSDN	an	Serial Data Detect Pair: Reserved for TI Manufacturing Test.
83	FSDP	an	Treat as a No Connect.

TABLE I

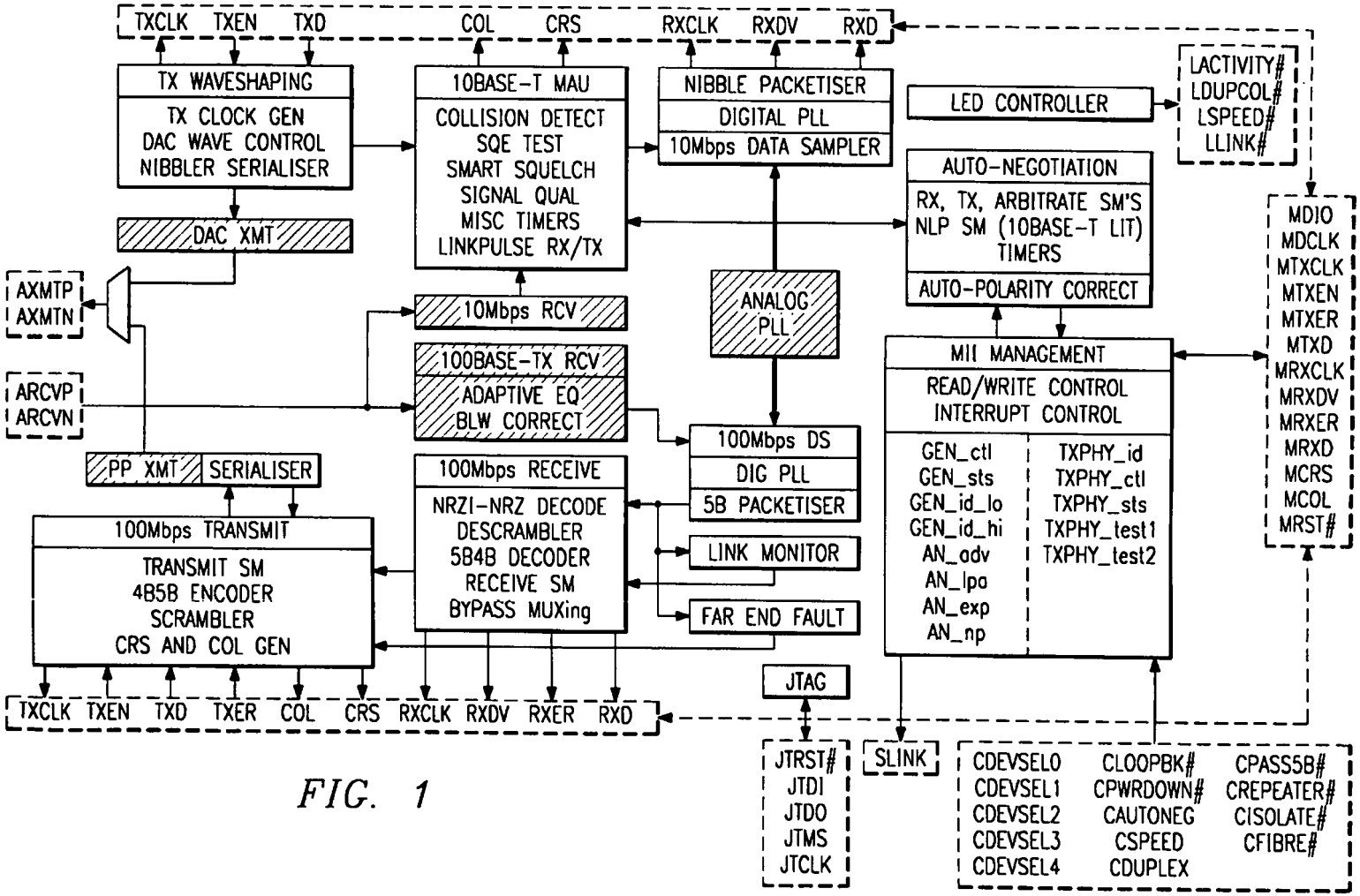
Network Interface Pins

Pin	Name	Type	Function
84	AVDD	supply	Power: Analog 3.3V supply connection.
85	ACT	an	Centre Tap: Connection to the primary centre-tap of the transmit transformer.
86	AGND	supply	Ground: Analog Ground connection.

TABLE I-continued

Network Interface Pins

Pin	Name	Type	Function
87	AXMTP	an	Transmit Pair: Differential line outputs from the device to the
88	AXMTN	an	transformer and termination components.
89	AGND	supply	Ground: Analog Ground connection.
90	AGND		
91	ARCVP	an	Receive Pair: Differential line inputs to the device from the
92	ARCVN	an	transformer and termination components.
93	AVDD	supply	Power: Analog 3.3V supply connection.
94	ATEST2	an	Analogue Test 2: A T.I. analogue test pin. Treat his pin as a no-connect (N/C).
95	ATEST3	an	Analogue Test 3: A T.I. analogue test pin. Treat his pin as a no-connect (N/C).
96	AVDD	supply	Power: Analog 3.3V supply connection.
97	N/C		No connect: Leave this pin unconnected.
98	ATEST4	an	Analogue Test 3: A.T.I. analogue test pin. Treat his pin as a no-connect (N/C).
99	AGND	supply	Ground: Analog Ground connection.
100	AGND		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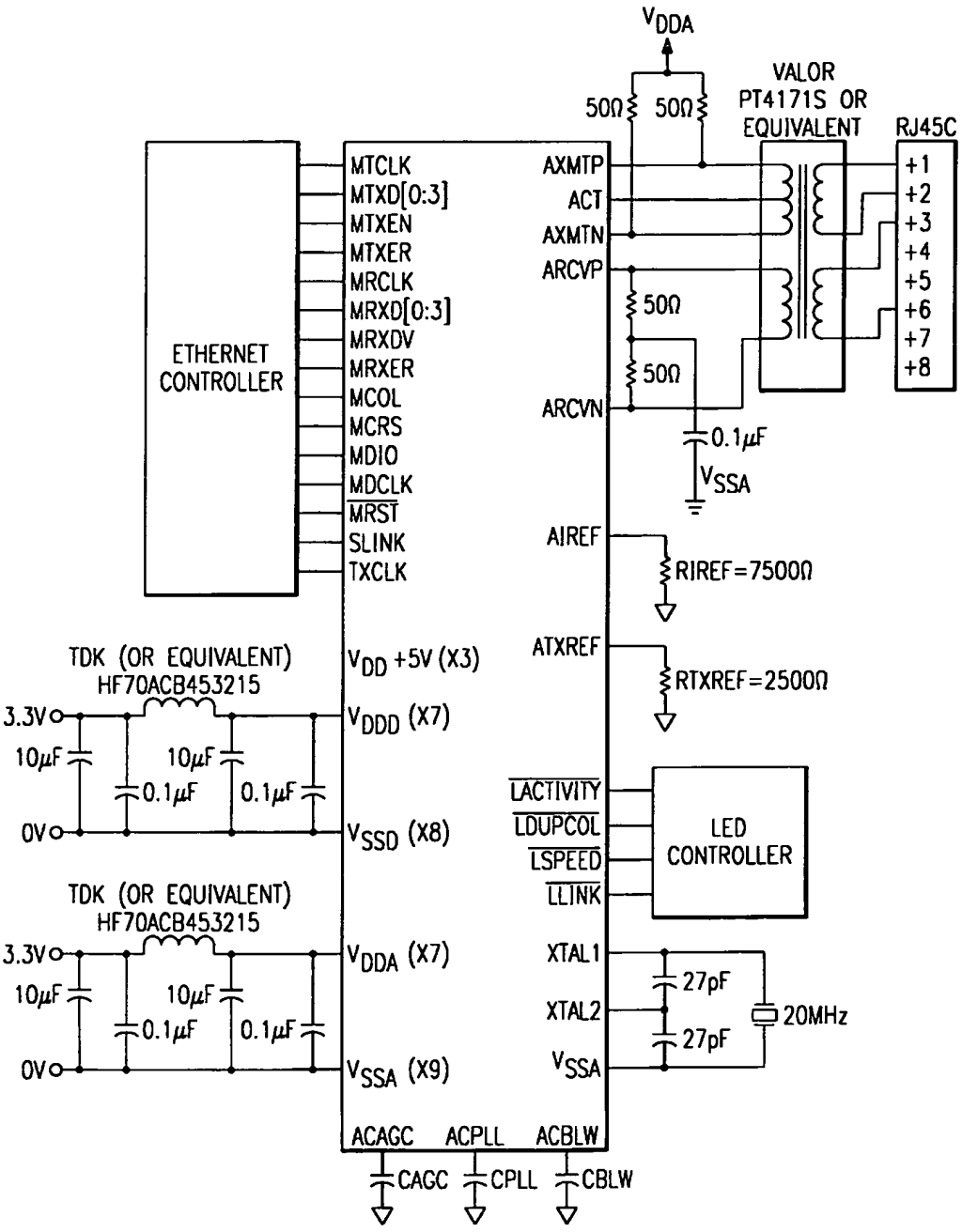
COL CRS
RXCLK RXDV RXD
TX WAVESHAPING
TX CLOCK GEN
DAC WAVE CONTROL
NIBBLER SERIALISER
DAC XMT
10BASE-T MAU
COLLISION DETECT
SQE TEST
SMART SQUELCH
SIGNAL QUAL
MISC TIMERS
LINKPULSE RX/TX
NIBBLE PACKETISER
DIGITAL PLL
10Mbps DATA SAMPLER
LED CONTROLLER
LACTIVITY#
LDUPCOL#
LSPEED#
LLINK#
AUTO-NEGOTIATION
RX, TX, ARBITRATE SM'S
NLP SM (10BASE-T LIT)
TIMERS
AUTO-POLARITY CORRECT
MDIO
MDCLK
MTXCLK
MTXEN
MTXER
MTXD
MRXCLK
MRXDV
MRXER
MRXD
MCRS
MCOL
MRST#
AXMTP
AXMTN
ARCVP
ARCVN
10Mbps RCV
100BASE-TX RCV
ADAPTIVE EQ
BLW CORRECT
ANALOG PLL
MII MANAGEMENT
READ/WRITE CONTROL
INTERRUPT CONTROL
GEN_ctl
GEN_sts
GEN_id_lo
GEN_id_hi
AN_adv
AN_lpa
AN_exp
AN_np
TXPHY_id
TXPHY_ctl
TXPHY_sts
TXPHY_test1
TXPHY_test2
PP XMT
SERIALISER
100Mbps DS
DIG PLL
5B PACKETISER
100Mbps RECEIVE
NRZI-NRZ DECODE
DESCRAMBLER
5B4B DECODER
RECEIVE SM
BYPASS MUXing
LINK MONITOR
FAR END FAULT
100Mbps TRANSMIT
TRANSMIT SM
4B5B ENCODER
SCRAMBLER
CRS AND COL GEN
JTAG
TXCLK TXEN TXD TXER COL CRS RXCLK RXDV RXER RXD
JTRST#
JTDI
JTDO
JTMS
JTCLK
SLINK
CDEVSEL0
CDEVSEL1
CDEVSEL2
CDEVSEL3
CDEVSEL4
CLOOPBK#
CPWRDOWN#
CAUTONEG
CSPEED
CDUPLEX
CPASS5B#
CREPEATER#
CISOLATE#
CFIBRE#

FIG. 1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50Ω
VALOR
PT4171S OR
EQUIVALENT
RJ45C
+1
+2
+3
+4
+5
+6
+7
+8
ETHERNET
CONTROLLER
MTCLK
MTXD[0:3]
MTXEN
MTXER
MRCLK
MRXD[0:3]
MRXDV
MRXER
MCOL
MCRS
MDIO
MDCLK
MRST
SLINK
TXCLK
AXMTP
ACT
AXMTN
ARCVP
50Ω
50Ω
ARCVN
0.1μF
VSSA
AIREF
RIREF=7500Ω
ATXREF
RTXREF=2500Ω
TDK (OR EQUIVALENT)
HF70ACB453215
3.3V
10μF
10μF
0.1μF
0.1μF
0V
VDD +5V (X3)
VDDD (X7)
VSSD (X8)
LACTIVITY
LDUPCOL
LSPEED
LLINK
LED
CONTROLLER
TDK (OR EQUIVALENT)
HF70ACB453215
3.3V
10μF
10μF
0.1μF
0.1μF
0V
VDDA (X7)
VSSA (X9)
XTAL1
XTAL2
VSSA
27pF
27pF
20MHz
ACAGC
ACPLL
ACBLW
CAGC
CPLL
CBLW

FIG. 2

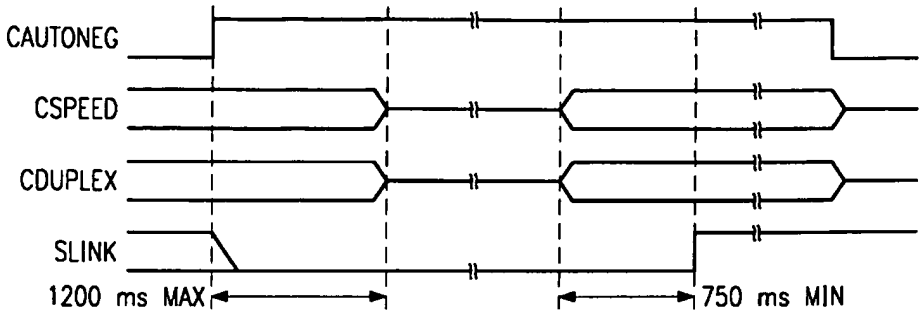


FIG. 3

GEN_ctl	GENERIC CONTROL REGISTER
GEN_sts	GENERIC STATUS REGISTER
GEN_id_hi	GENERIC IDENTIFIER (HIGH)
GEN_id_lo	GENERIC IDENTIFIER (LOW)
AN_adv	AUTO-NEGOTIATION ADVERTISEMENT
AN_lpa	AUTO-NEGOTIATION LINK-PARTNER ABILITY
AN_exp	AUTO-NEGOTIATION EXPANSION
AN_np	AUTO-NEGOTIATION NEXT-PAGE TRANSMIT
RESERVED	
RESERVED	RESERVED BY IEEE 802.3
RESERVED	
TXPHY_id	PHY IDENTIFIER
TXPHY_ctl	PHY CONTROL REGISTER
TXPHY_sts	PHY STATUS REGISTER

FIG. 4

START DELIMITER	OPERATION CODE	PHY ADDRESS	REG ADDRESS	TURN-AROUND	DATA
01	10	AAAAA	RRRRR	Z0	DDDD.DDDD.DDDD.DDDD

FIG. 5A

START DELIMITER	OPERATION CODE	PHY ADDRESS	REG ADDRESS	TURN-AROUND	DATA
01	01	AAAAA	RRRRR	10	DDDD.DDDD.DDDD.DDDD

FIG. 5B

PHY GENERIC CONTROL REGISTER - GEN_ctl

BYTE1								BYTE0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET	LOOPBK	SPEED	AUTONEG	PDOWN	ISOLATE	AUTORSRT	DUPLEX	COLTEST	RESERVED						

FIG. 6

PHY GENERIC STATUS REGISTER - GEN_sts

BYTE1										BYTE0					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	1	RESERVED				1	AUTOCMPLT	RFAULT	1	LINK	JABBER	1

FIG. 7

PHY GENERIC IDENTIFIER - GEN_id_hi/GEN_id_lo

BYTE1															BYTE0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ORGANISATIONALLY UNIQUE IDENTIFIER (OUI) BITS 3-18															
OUI BITS 19-24										MANUFACTURER MODEL NUMBER					MANUFACTURER REVISION NUMBNER

FIG. 8

AUTO-NEGOTIATION ADVERTISEMENT REGISTER - AN_adv

BYTE1															BYTE0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NP	RES	RF	TECHNOLOGY ABILITY FIELD								SELECTOR FIELD				

FIG. 9

AUTO-NEGOTIATION LINK PARNTER ABILITY REGISTER – AN_lpa

BASE PAGE ENCODING

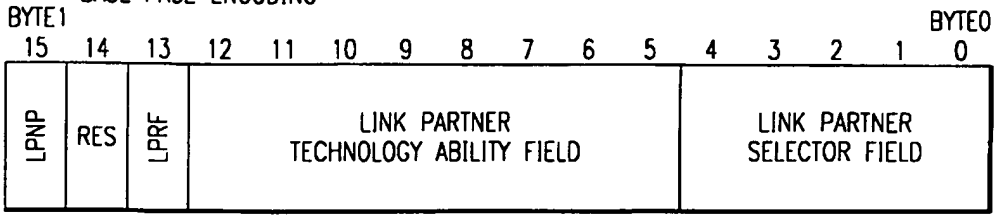


FIG. 10A

MESSAGE PAGE ENCODING (LPMP=1)

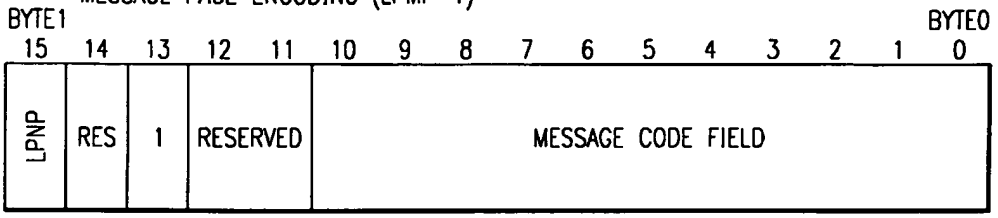


FIG. 10B

UNFORMATTED PAGE ENCODING (LPMP=0)

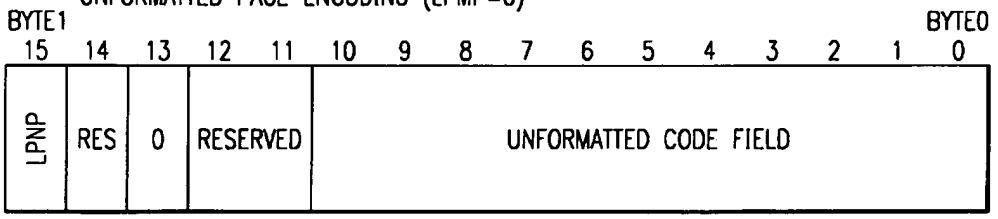


FIG. 10C

AUTO-NEGOTIATION EXPANSION REGISTER – AN_exp

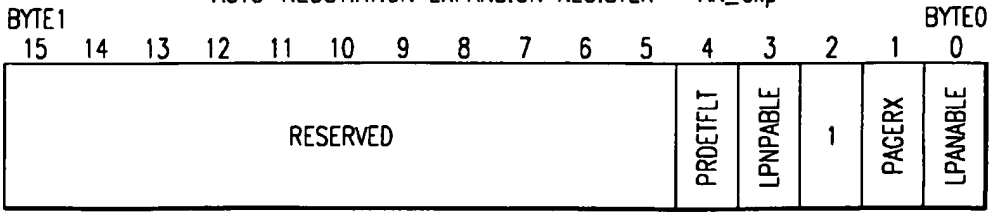


FIG. 11

AUTO-NEGOTIATION NEXT PAGE TRANSMIT REGISTER - AN_np

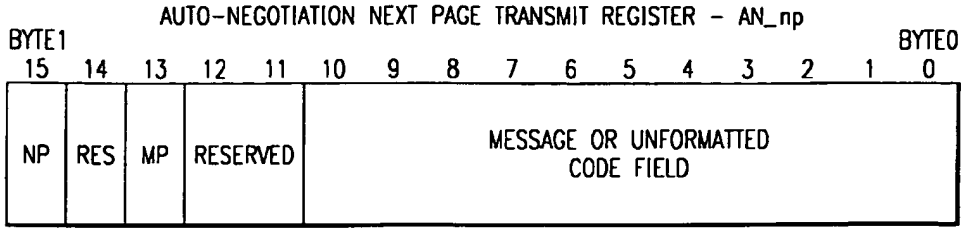


FIG. 12

TLAN PHY IDENTIFIER HIGH/LOW - TLPHY_id

0x0003

FIG. 13

TLAN PHY CONTROL REGISTER - TLPHY_ctl

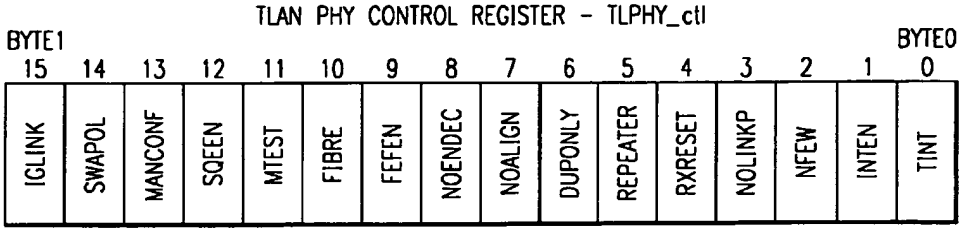


FIG. 14

TLAN PHY STATUS REGISTER - TLPHY_sts

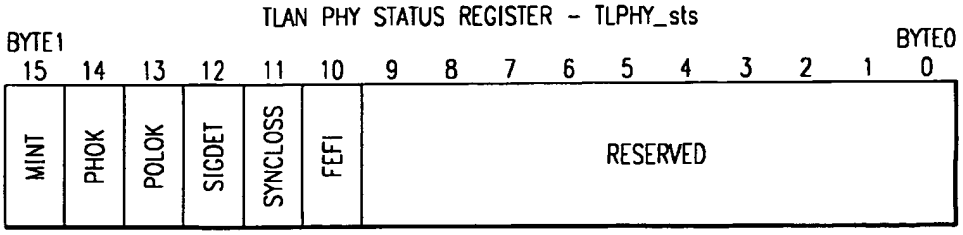


FIG. 15

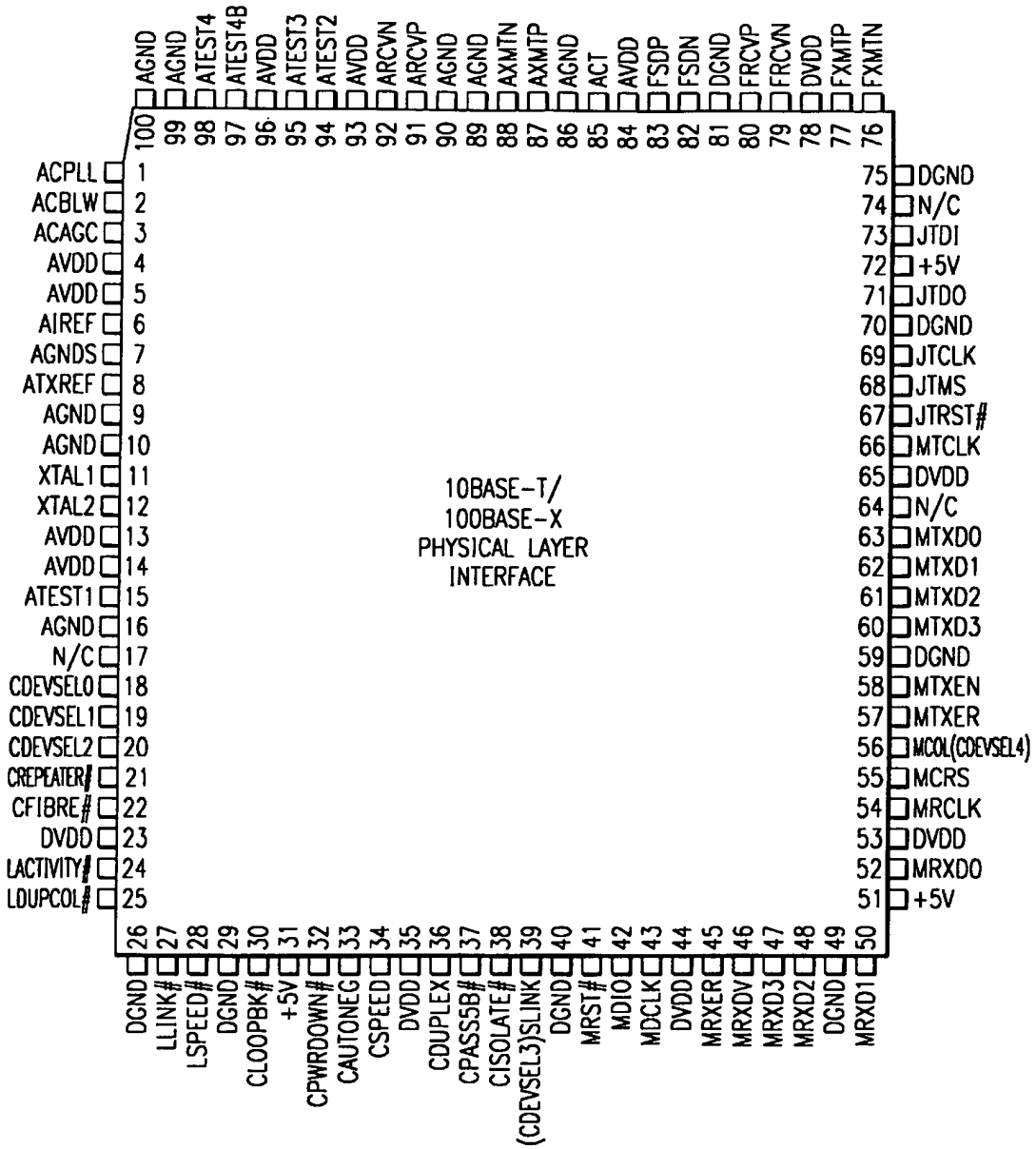
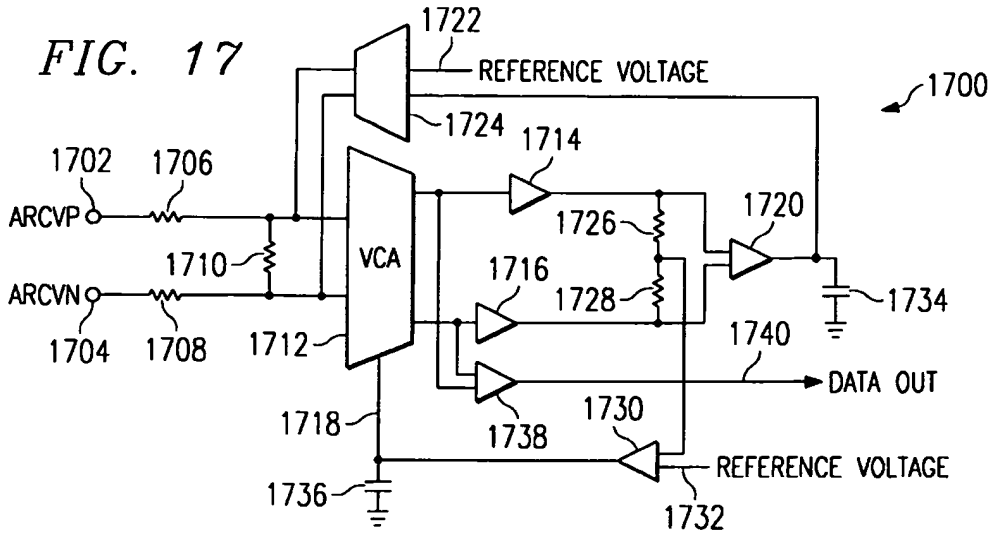


FIG. 16

KEY TO PIN NAME PREFIXES:

- D SUPPLY OR GROUND FOR DIGITAL LOGIC
- A SUPPLY OR GROUND FOR ANALOGUE CIRCUITRY
- C CONFIGURATION MODES
- M MEDIA INDEPENDENT INTERFACE CONNECTION
- L EXTERNAL LED'S
- J JTAG-TEST PORT
- F INTERFACE TO FIBRE TRANSCEIVER MODULE
- S INDICATING PHY STATUS
- A CONNECTIONS TO THE INTERNAL ANALOGUE CIRCUITRY

FIG. 17


1722
REFERENCE VOLTAGE
1700
1724
1714
1702
1706
ARCVP
1720
1726
VCA
1710
1716
1728
1734
ARCVN
1740
1704
1708
1712
DATA OUT
1730
1718
1738
REFERENCE VOLTAGE
1736
1732

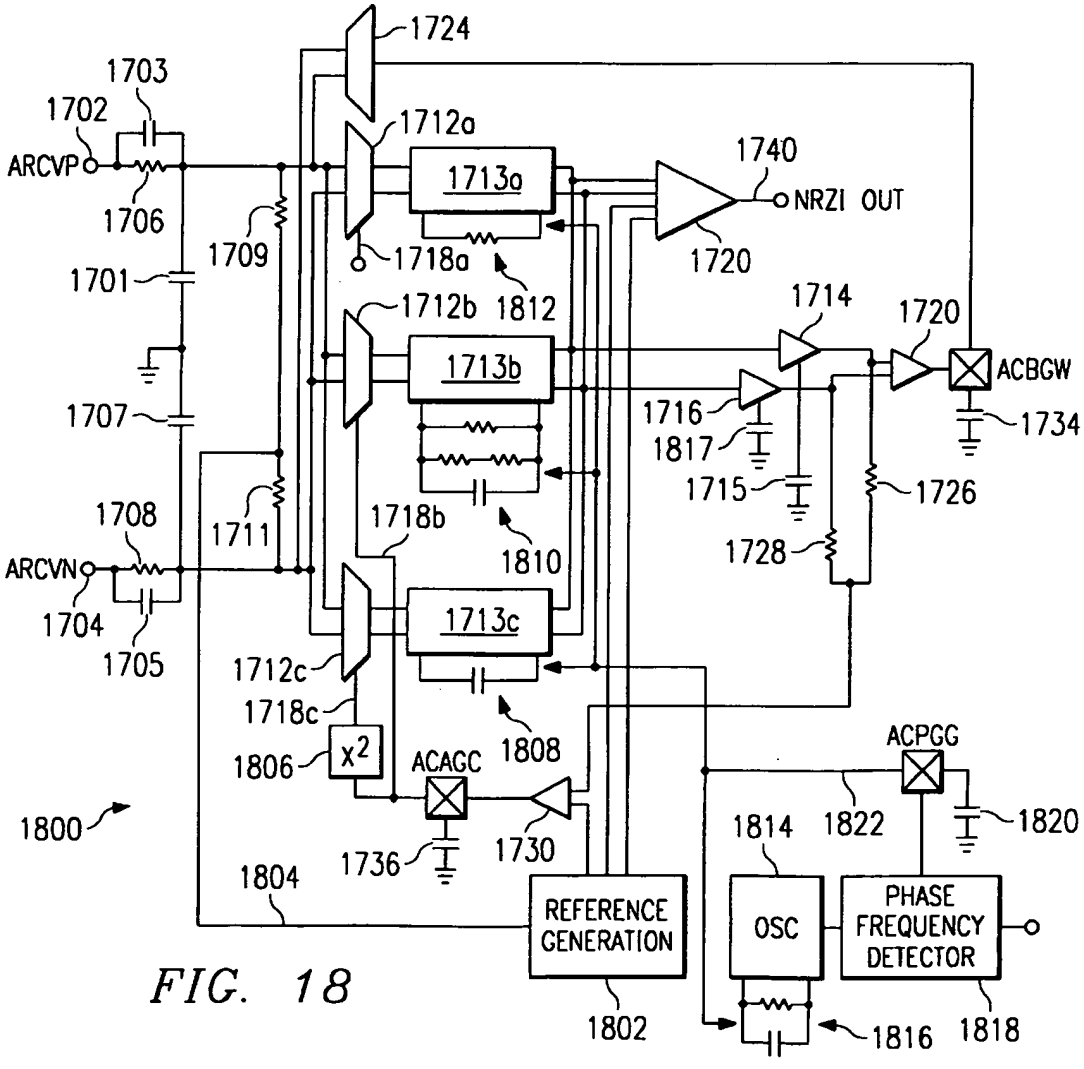

1724
1703
1702
1712a
1740
ARCVP
1713a
NRZI OUT
1706
1709
1718a
1720
1701
1712b
1812
1714
1720
1713b
ACBGW
1716
1734
1707
1817
1715
1726
1708
1711
1718b
1728
1810
ARCVN
1704
1713c
1705
1712c
1718c
1808
ACPGG
1806
X2
ACAGC
1822
1820
1800
1814
1730
1736
1804
REFERENCE GENERATION
OSC
PHASE FREQUENCY DETECTOR
1802
1816
1818

FIG. 18

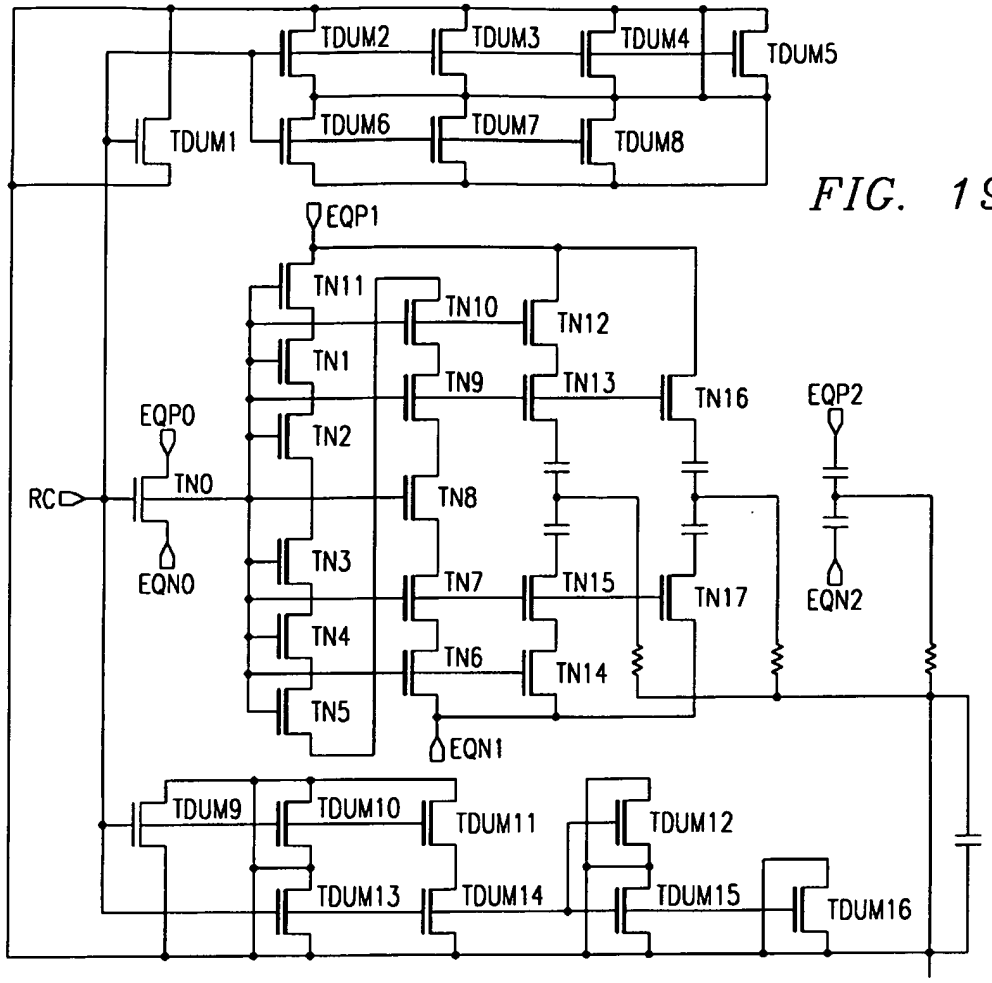

TDUM2
TDUM3
TDUM4
TDUM5
TDUM1
TDUM6
TDUM7
TDUM8
EQP1
TN11
TN10
TN12
TN1
TN9
TN13
TN16
EQP2
EQP0
TN2
RC
TN0
TN8
EQN0
TN3
TN7
TN15
TN17
EQN2
TN4
TN6
TN14
TN5
EQN1
TDUM9
TDUM10
TDUM11
TDUM12
TDUM13
TDUM14
TDUM15
TDUM16

FIG. 19

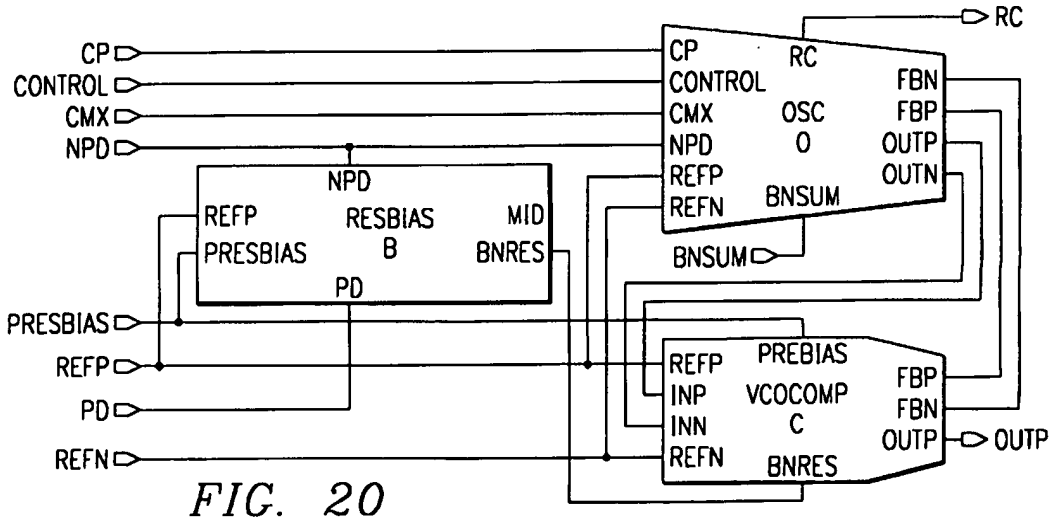

RC
CP
CONTROL
CMX
NPD
CP
RC
CONTROL
FBN
CMX
OSC
FBP
NPD
0
OUTP
REFP
OUTN
REFN
BNSUM
NPD
REFP
RESBIAS
MID
PRESBIAS
B
BNRES
PD
BNSUM
PRESBIAS
REFP
PD
REFN
PREBIAS
REFP
FBP
INP
VCOCOMP
FBN
INN
C
OUTP
OUTP
REFN
BNRES

FIG. 20

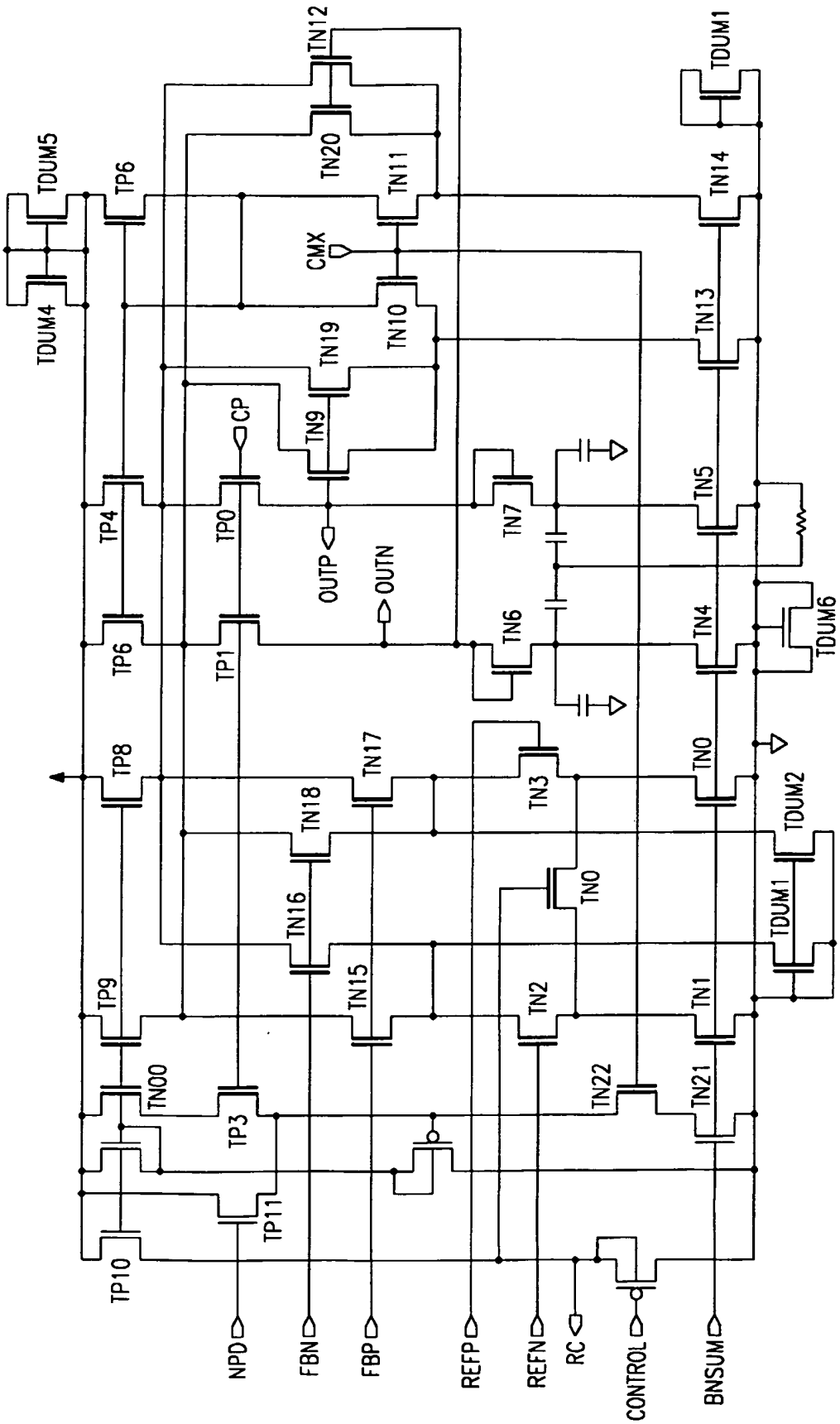

TDUM5
TP6
TN12
TN20
TN11
TDUM1
TN14
CMX
TDUM4
TN19
TN10
TN13
CP
TN9
TP4
TP0
TN7
TN5
OUTP
OUTN
TP6
TP1
TN6
TN4
TDUM6
TP8
TN17
TN3
TN0
TDUM2
TN18
TN0
TN16
TDUM1
TP9
TN15
TN2
TN1
TN00
TP3
TN22
TN21
TP11
TP10
NPD
FBN
FBP
REFP
REFN
RC
CONTROL
BNSUM

FIG. 21

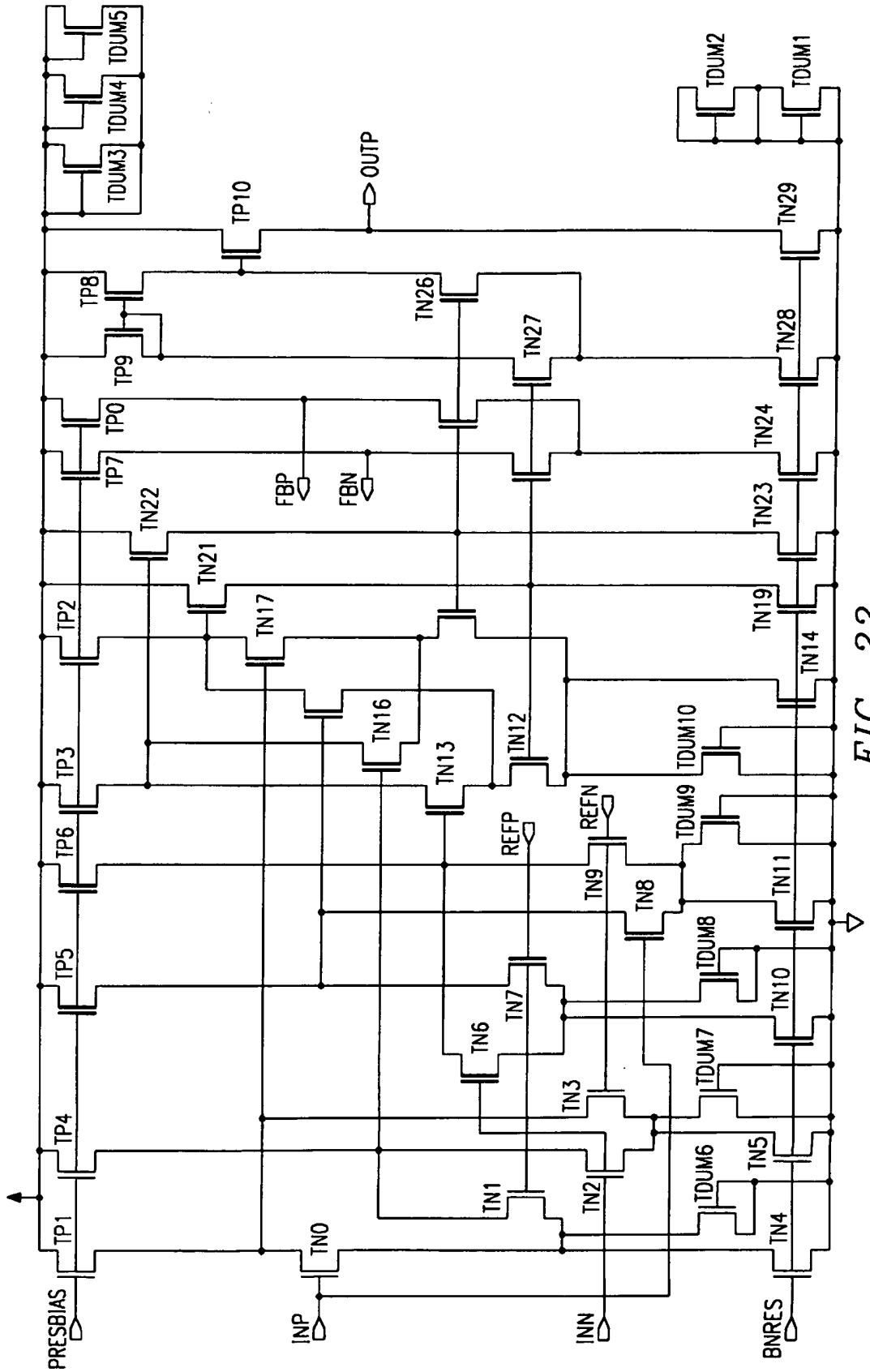

PRESBIAS
INP
INN
BNRES
TP1
TP4
TP5
TP6
TP3
TP2
TP7
TP0
TP9
TP8
TP10
TN0
TN1
TN2
TN3
TN4
TN5
TN6
TN7
TN8
TN9
TN10
TN11
TN12
TN13
TN14
TN16
TN17
TN19
TN21
TN22
TN23
TN24
TN26
TN27
TN28
TN29
TDUM1
TDUM2
TDUM3
TDUM4
TDUM5
TDUM6
TDUM7
TDUM8
TDUM9
TDUM10
REFP
REFN
FBP
FBN
OUTP

FIG. 22

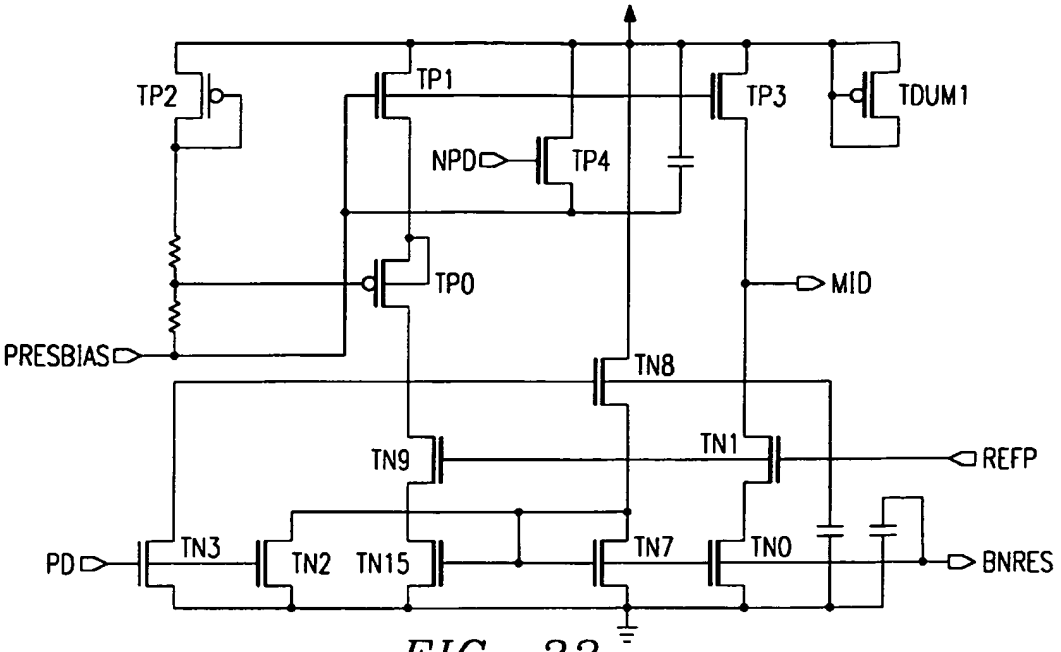

TP2
TP1
TP3
TDUM1
NPD
TP4
TP0
MID
PRESBIAS
TN8
TN9
TN1
REFP
PD
TN3
TN2
TN15
TN7
TN0
BNRES

FIG. 23

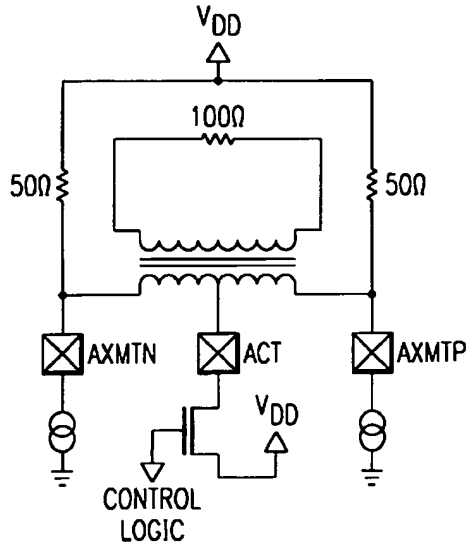

VDD
100Ω
50Ω
50Ω
AXMTN
ACT
AXMTP
VDD
CONTROL
LOGIC

FIG. 25

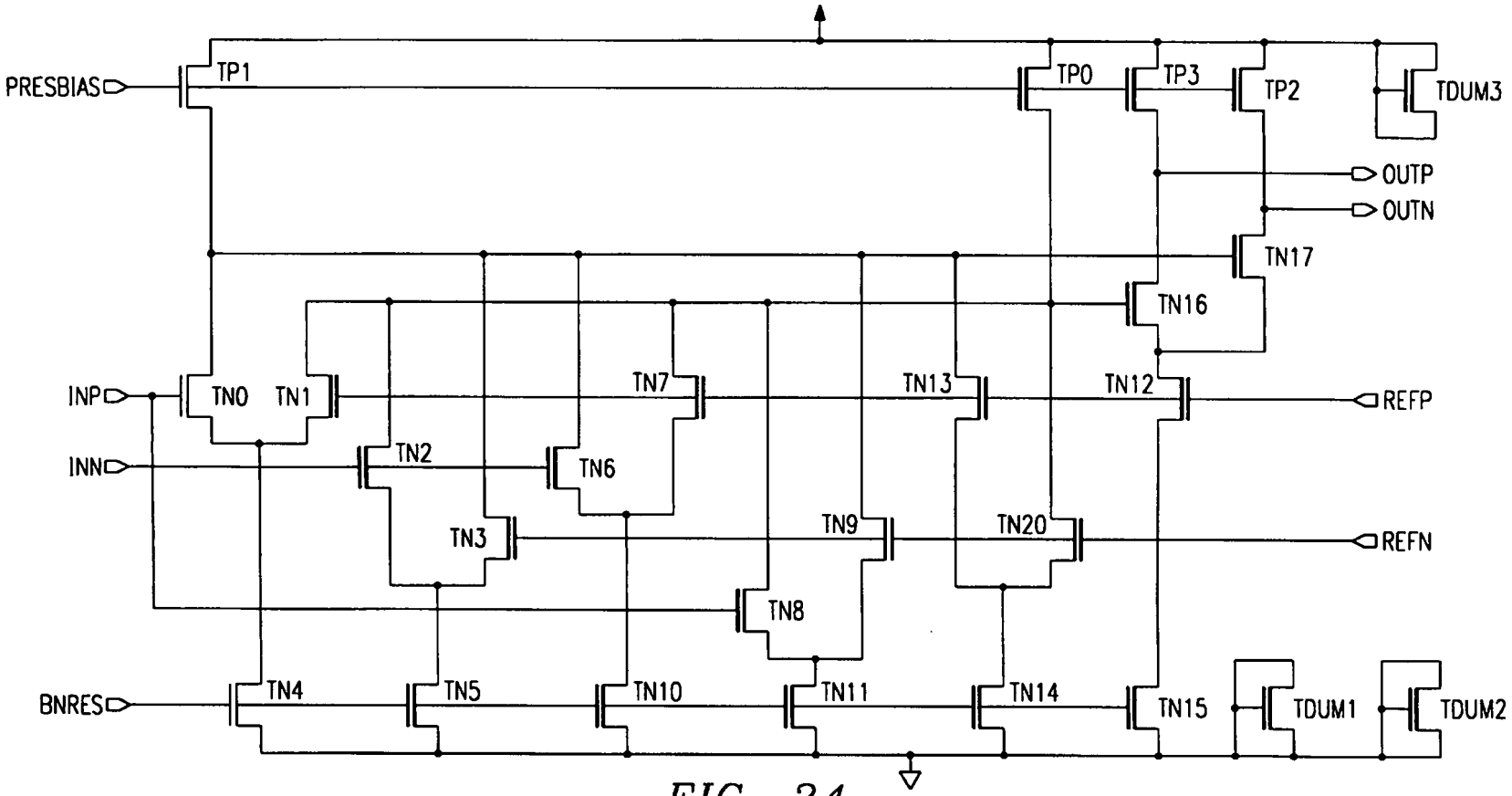

PRESBIAS
TP1
TP0
TP3
TP2
TDUM3
OUTP
OUTN
TN17
TN16
INP
TN0
TN1
TN7
TN13
TN12
REFP
INN
TN2
TN6
TN3
TN9
TN20
REFN
TN8
BNRES
TN4
TN5
TN10
TN11
TN14
TN15
TDUM1
TDUM2

FIG. 24

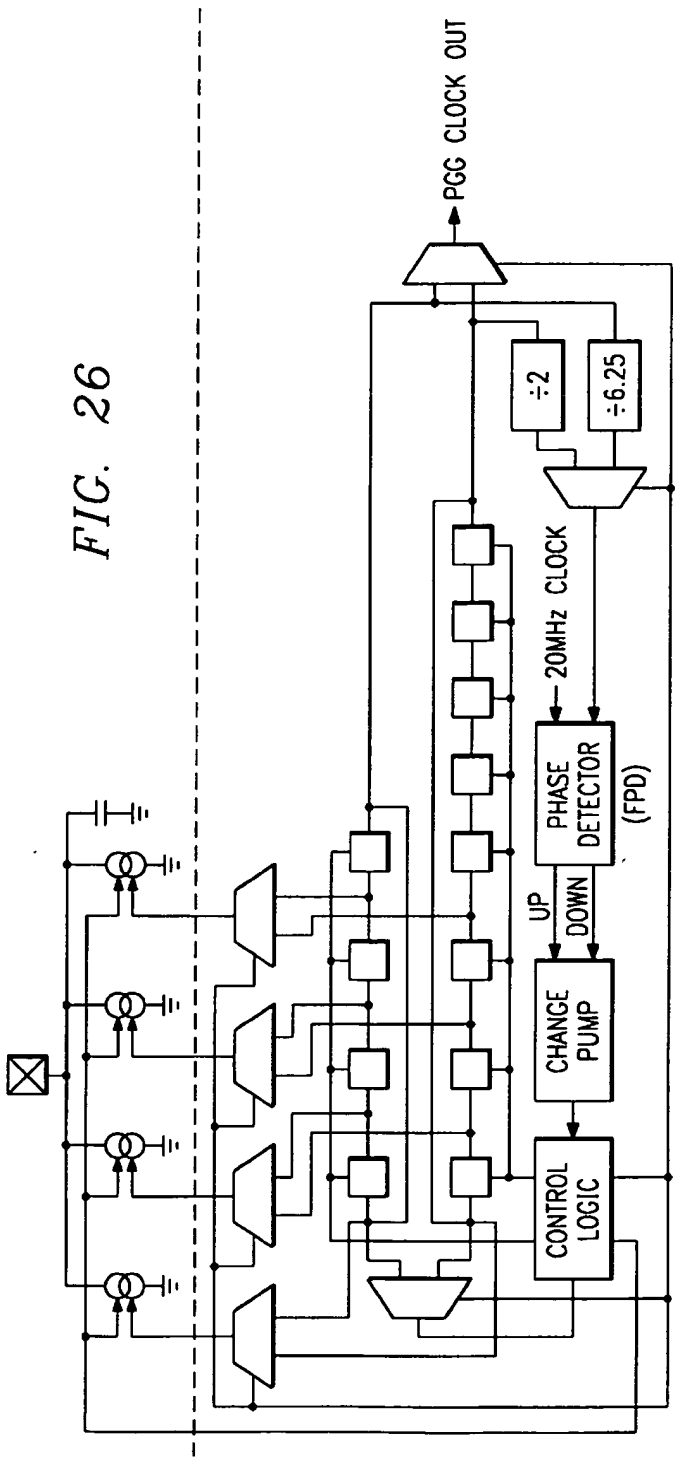

PGG CLOCK OUT
÷2
÷6.25
20MHz CLOCK
PHASE DETECTOR
(FPD)
UP
DOWN
CHANGE PUMP
CONTROL LOGIC

FIG. 26

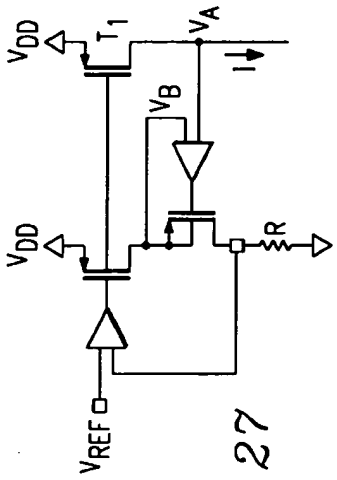
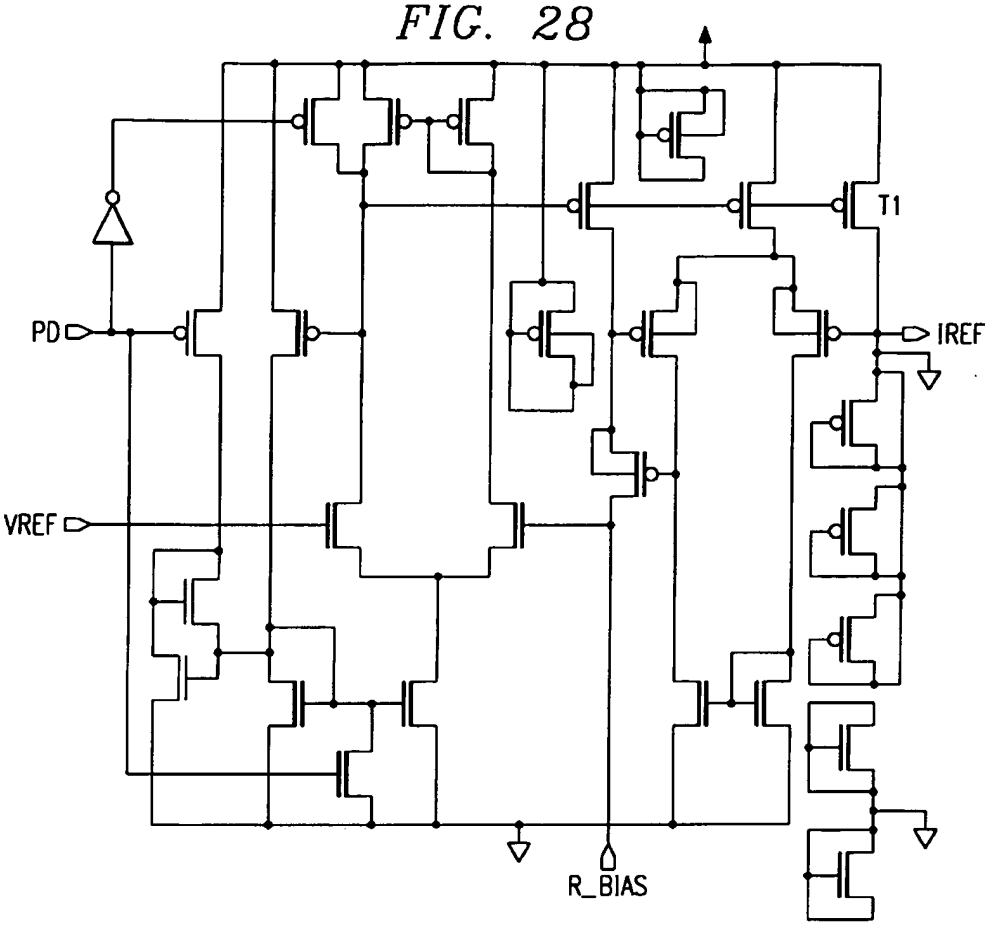

V_{DD}
T_1
V_A
I
V_B
V_{DD}
R
V_{REF}

FIG. 27

FIG. 28


T1
PD
IREF
VREF
R_BIAS

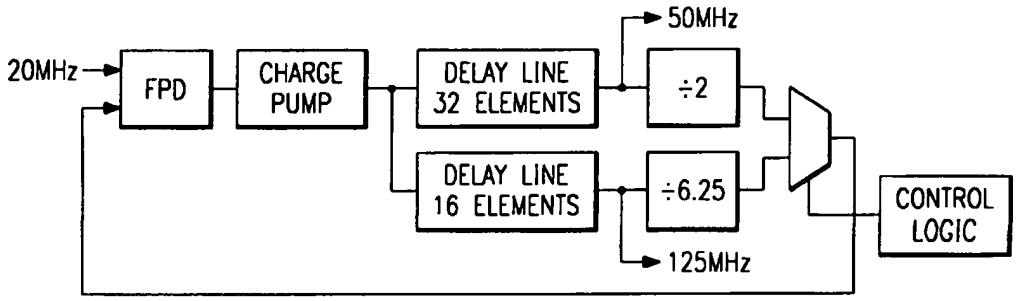

20MHz
FPD
CHARGE PUMP
DELAY LINE 32 ELEMENTS
DELAY LINE 16 ELEMENTS
÷2
÷6.25
50MHz
125MHz
CONTROL LOGIC

FIG. 29